

H2ID Heatmap Wizard

Interactive Design-Space Exploration for RF Power Amplifiers

The *H2ID* Heatmap Wizard provides a visual and interactive approach to RF power amplifier design. Rather than evaluating a single operating condition at a time, the wizard exposes the entire *H2ID* design space and shows how performance varies across it. The wizard allows engineers to explore hundreds of candidate operating points simultaneously and rapidly identify the most promising regions of the design space.

Using color-coded heatmaps, designers can instantly identify regions of high efficiency, favourable power factor, high output power, acceptable voltage stress, desired conduction angle, or reduced knee interaction and degradation. Practical device constraints can be applied and modified in real time, allowing immediate exploration of design trade-offs.

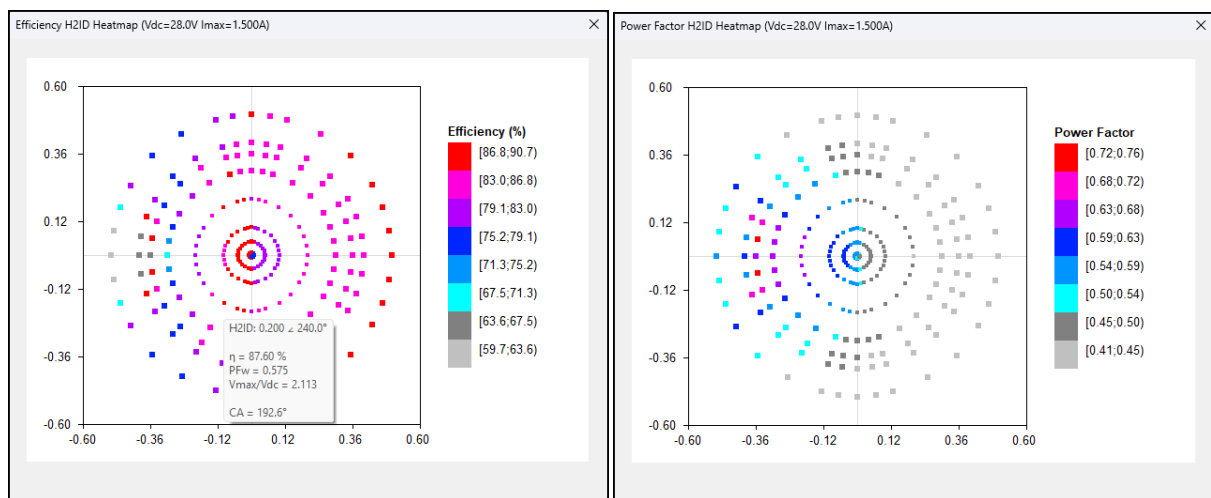


Figure 1. Efficiency and Power Factor heatmaps. Tooltips are shown when the mouse is moved over a *H2ID* operating point. The tooltip shown is with the transistor knee ignored.

The *H2ID* Heatmap Wizard enables users to:

- Visualize the complete *H2ID* design space.
- Identify operating regions that provide the best compromise between efficiency, power output, power factor, voltage stress and current utilization without pushing into the transistor knee boundary.
- Apply realistic transistor operating constraints.
- Inspect individual operating points in detail.
- Display intrinsic dynamic load lines and the associated intrinsic or external harmonic load impedances (Z_{Li} ; Z_{Le}).
- Compare multiple operating points simultaneously.
- Perform real-time "what-if" analysis using interactive slider controls.

The wizard maps each *H2ID* vector in the design space to the associated normalized intrinsic output current waveform. For each *H2ID* operating point, a complementary normalized voltage waveform is synthesized to maximize waveform efficiency. The voltage waveform is limited to the fundamental, second, and third harmonics, and negative resistance is not permitted. With the waveforms defined, the intrinsic normalized harmonic load impedances are known.

The output power is determined by the selected complementary waveform pair, the associated power factor, the targeted peak current and the applied *dc* voltage. The transistor knee then introduces an important practical trade-off between output power and efficiency. At the peak power point, efficiency

is seriously degraded by the transistor knee. As the targeted peak current is reduced, output power decreases, but efficiency improves towards the waveform efficiency.

When a specific transistor is targeted, the normalized current waveform is scaled to the peak level targeted, while the voltage waveform is scaled to just touch the knee boundary with the dc voltage specified. With the scale factors known, the associated intrinsic harmonic load impedances can be calculated. If a transistor model is available or the parasitic output side components are known, the intrinsic load impedances can be mapped to the external reference plane. To summarize:

$H2ID$ vector $\rightarrow$ Normalized intrinsic output current waveform $\rightarrow$ Normalized complementary voltage waveform $\rightarrow$ Current scaled to specified peak $\rightarrow$ Voltage scaled to touch the knee boundary with the dc voltage as specified $\rightarrow$ Scale factors known $\rightarrow$ Intrinsic harmonic load impedances known $\rightarrow$ External harmonic load impedances obtained.

Up to six operating points in the $H2ID$ vector space can be inspected simultaneously, allowing direct comparison of efficiency, power factor, output power, conduction angle, harmonic load impedances, voltage stress, current utilization, knee factor, and dynamic load-line behaviour. Persistent inspectors allow selected designs to be retained while device parameters and design constraints are changed, making before-and-after comparisons immediate. The inspector operating points and window positions can be cleared by using the option provided when the heatmap and device parameters are specified.

The knee boundary can be either linear (constant knee resistance) or curved. Up to eight points can be specified to define the curvature. Linear interpolation is used between adjacent points. The points can be positioned to obtain a tight piecewise-linear fit to the transistor knee characteristic. Operation beyond the knee boundary, including waveform clipping and compression, is not considered. The Wizard determines the maximum unclipped operating condition. The saturated power for a Class-B-like or Class-F-like operating point is typically a few decibels higher than the maximum unclipped output power calculated in the wizard.

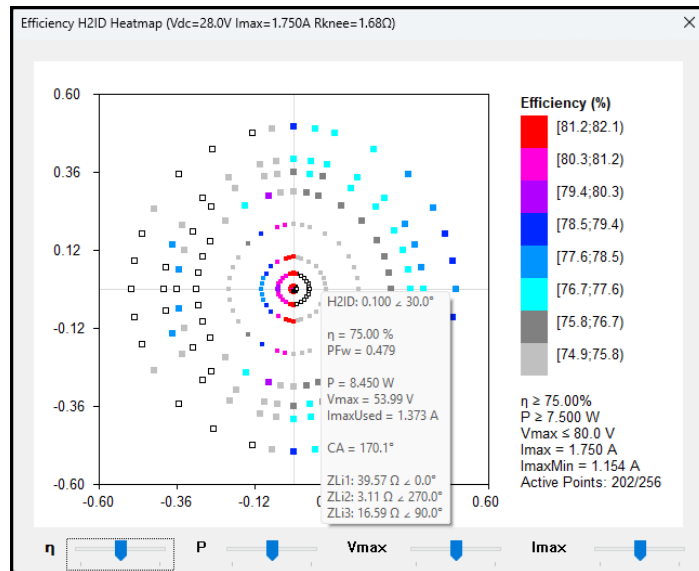


Figure 2. The effect of the transistor knee on efficiency is shown here. Constraint sliders allow acceptable efficiency, power, voltage and current limits to be adjusted interactively.

The dynamic load lines displayed in the inspectors provide visual validation of the waveform synthesis. The load line remains outside the knee region and touches the knee boundary at the point implied by the waveform solution. The dynamic load line plot therefore allows the designer to verify both the synthesized waveform behaviour and the associated transistor constraints immediately.

A cascade network consisting of up to three shunt capacitors and three series inductors is used to map the intrinsic load impedances to the external reference plane. In the Ampsa Amplifier Design Wizard, the mapping can be done by using power parameters. Other than linearity, no assumptions are made when the power parameters are used (internal feedback and resistive losses are allowed).

Instead of asking only what load impedance satisfies a particular design condition, the *H2ID* Heatmap Wizard allows the designer to see which regions of the available design space satisfy the required efficiency, power, voltage and current constraints, and then obtain the harmonic terminations required to realize a selected solution.

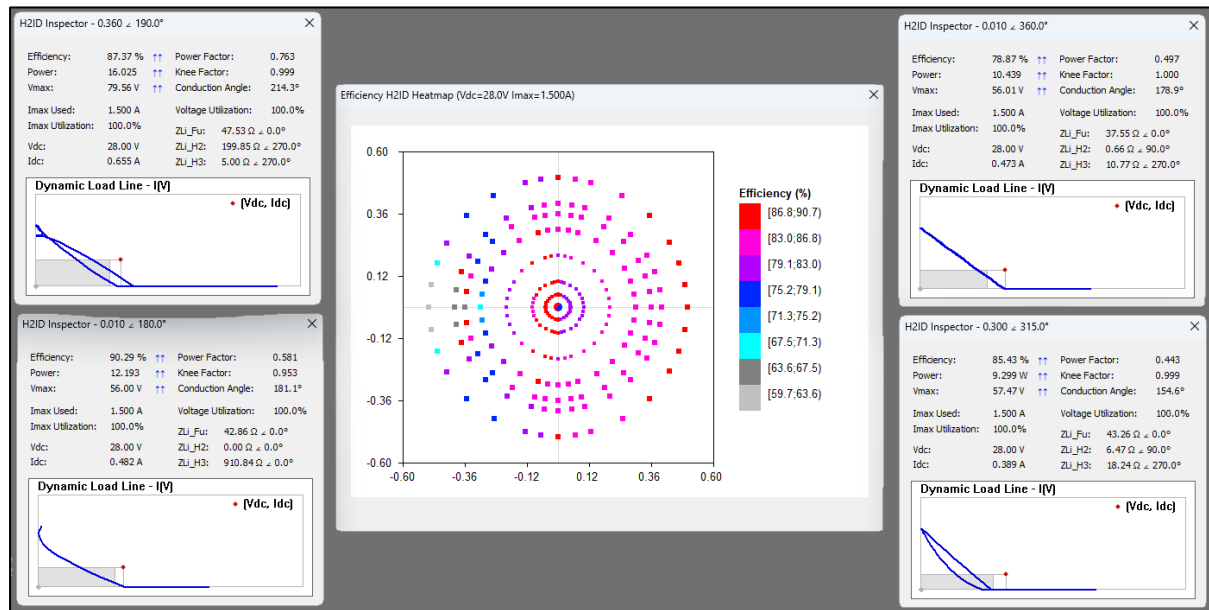


Figure 3. Inspectors can be opened for up to six operating points in the *H2ID* design space. The knee was ignored here. The red dots show the *dc* operating points. The shaded rectangles show the output power relative to the *dc* power.

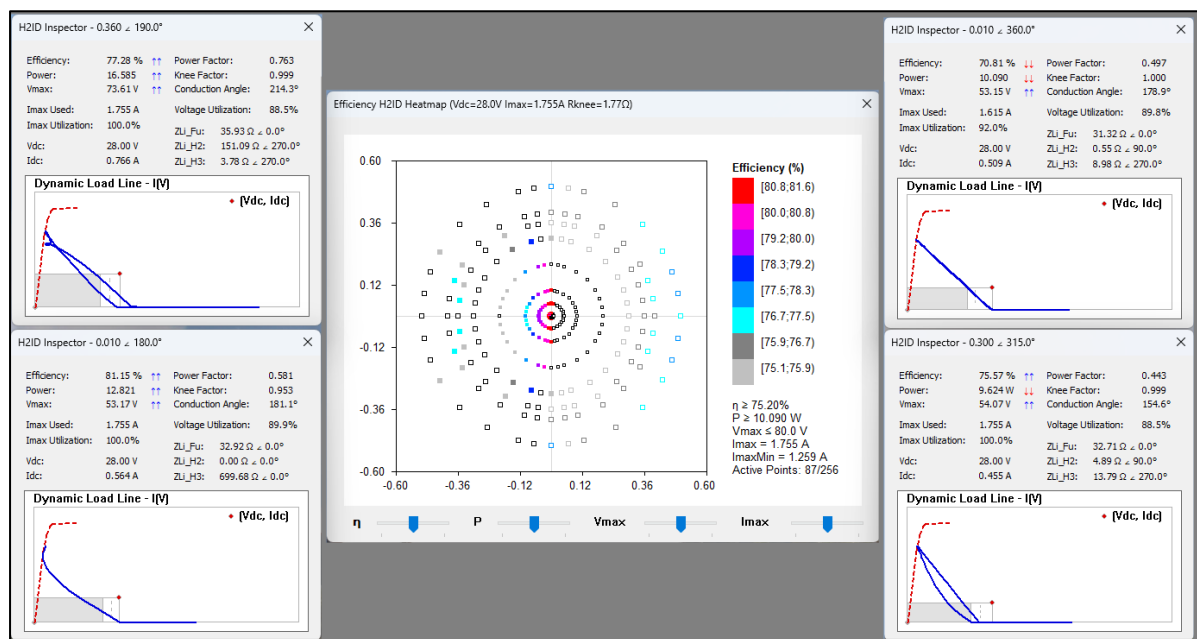


Figure 4. The same inspectors as in Figure 3 were used here, but the degrading effect of the knee is considered here. The dashed red lines show the knee boundary. Note the red arrows used when the performance is off target.

H2ID Heatmap Wizard Specifications and Parameters

H2ID maximum: 0.6
[0.1; 0.2; 0.3; 0.4; 0.5; 0.6]

Marker scale factor: 1
[0.5; 2.0]

Heatmap (HM) Options

- ☒ Efficiency
- ☐ Power or PFW
- ☐ Efficiency x PFW
- ☐ Vmax/Vdc
- ☐ Conduction Angle
- ☐ Knee Factor (KF)
- ☐ Imax_Used/Imax
- ☒ Auto Range
- ☒ Show Rejected
- ☐ Delete Inspector Data

Imax: Maximum drain current
PFW: Power Factor

OK Cancel Help

I/V-plane Constraints and Device Parameters

☐ Ignore I/V-plane Constraints

Drain DC Voltage (Vdc): 28.00 V

Imax (Target): 1.500 A

Tune: ☒ Imax ☐ Vdc ☐ RSB

Knee Boundary

☒ Linear ☐ Curved

Knee Segments

Knee Resistance (RSB): 1.68 Ohm
(0 ≤ RSB < Vdc/Imax)

Parasitic Components (ZLi to ZLe)

CP1 (pF)	SL1 (nH)	CP2 (pF)	SL2 (nH)	CP3 (pF)	SL3 (nH)
1.170	0.550	0.250	0.100	0.250	0.100

ZLi to ZLe Frequencies (GHz)

Lowest Frequency (FL): 1.00000 Highest Frequency (FH): 3.80000 Frequency Increment (FI): 0.28000

☐ Show ZLexternal at FH Up to 11 frequencies are allowed.

Design Filters

- ☒ Constrain Efficiency Minimum Efficiency: 75.0 (%)
- ☒ Constrain Output Power Minimum Power: 10.000 (W)
- ☒ Constrain Drain Voltage (Vmax) Maximum Voltage: 80.0 (V)
- ☒ Trade Excess Power for Efficiency

Figure 5. The heatmap and device parameters, the design filters provided and the heatmap options are shown here.

The controls for the wizard are shown in Figure 5. Note that the marker size and the $H2ID$ range can be adjusted. When the Show Rejected heatmap option is selected, hollow markers are used at $H2ID$ operating points not meeting the targets set. When this option is not selected, the relevant markers are not shown.

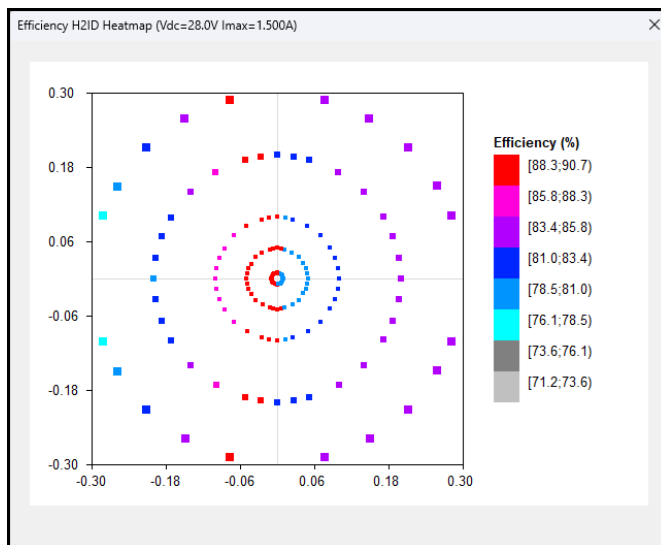


Figure 6. The $H2ID$ range was reduced from 0.6 to 0.3 in this example. Note the Class-F-like and Class-B-like efficiency at low distortion levels.

When the knee boundary is set and the Trade Excess Power option is selected, excess power is traded for out-of-range efficiency by lowering the targeted maximum current (reduced current utilization).

The $H2ID$ Heatmap Wizard transforms RF power-amplifier design from a search for a single optimum solution into an interactive exploration of the feasible design space. The designer can identify, inspect and compare practical solutions before selecting the harmonic terminations required for implementation.