Introduction to the Ampsa ADW

The ADW is a synthesis tool for single-ended RF and microwave amplifiers and impedance-matching networks. While matching can be to an external reference plane, the focus in the ADW is on controlling the intrinsic load terminations.

If a harmonic-balance simulator is available, it should be used to verify the performance of an amplifier designed in the ADW. Considerable effort went into the development of the ADW to minimize the discrepancies.

EM simulation of the matching networks designed in the ADW is advised. EM optimization can be used to resolve any discrepancies. It is generally good practice to use *S*-parameter based models for the microstrip junctions in the final phase of an ADW design.

A structured design approach is followed in the ADW. The diagram shown in Figure 1 provides an overview of the functionality provided in the Analysis Module of the ADW. ADW circuits can be analysed, tuned, and optimized in the Analysis Module. The analysis options include standard analysis, loop-gain analysis, as well as reflection analysis. ADW schematics can be exported in DXF format or as a basic script (.bas). The ADW artwork can be exported in DXF or HPGL format, as a basic script or in Sonnet Software® format (.son). The basic scripts are used for exports to Microwave Office™.

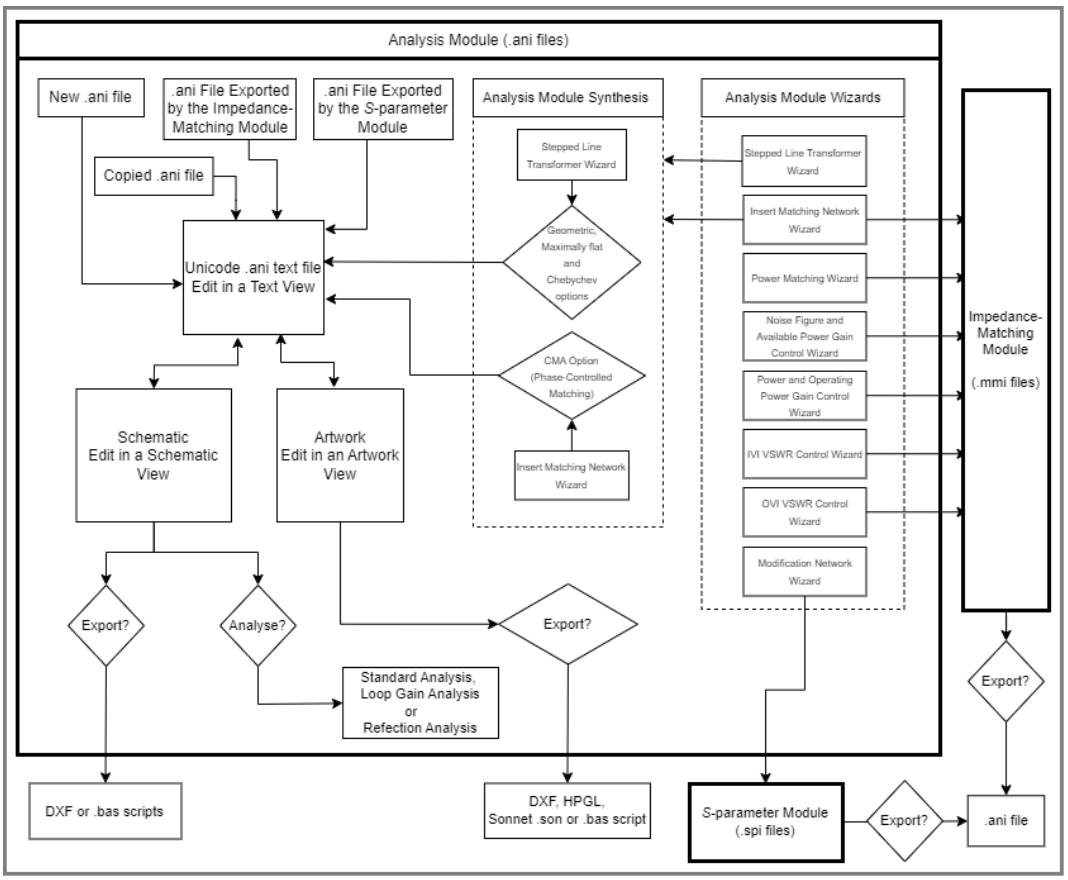

Figure 1. Overview of the Functionality Provided in the Analysis Module of the Amplifier Design Wizard.

Wizards are provided in the Analysis Module for various purposes. Some of the wizards are used to setup impedance-matching problems to be solved with the Impedance-Matching module (.mmi files). The networks associated with two of the wizards are synthesized directly in the Analysis Module (Stepped-line Transformers and phase-controlled matching networks).

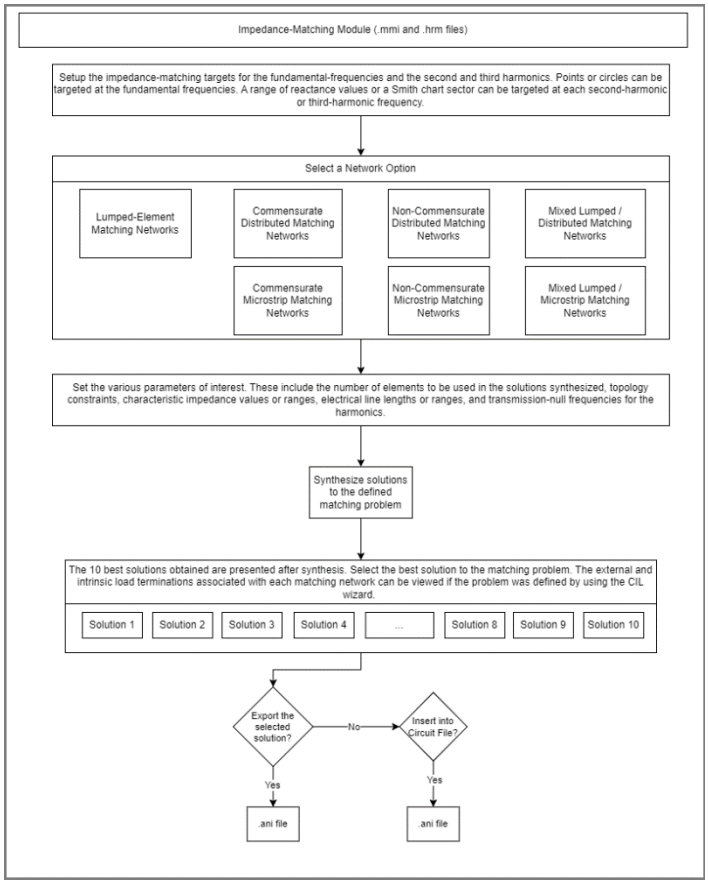

Figure 2. The design flow in the Impedance-Matching Wizard.

A wizard is also provided for setting up the specifications for a modification network (A lossy network used for gain control, improving the stability, and improving the VSWRs before matching). Modification networks can be synthesized in the *S*-parameter Module. The *S*-parameter and noise parameter date are stored in .spi files. The design flow in the S-parameter module is illustrated in Figure 3.

The *S*-parameter module is also used to fit transistor models. The first step in this process is to fit a linear model to a set of broadband *S*-parameters. The fitted model is used to map the intrinsic load terminations to the external terminations, and vice versa. (It is also used for extrapolation purposes.) The class of operation, the *dc* operating point, *I*/*V*-plane boundary lines for the intrinsic load lines and the harmonic content associated with the specified class of operation must also be specified to complete the modeling process. Mode switching is allowed in the ADW. ADW models are stored in .mdl files.

When a model has been fitted to the transistor, power contours and maximum-efficiency lines can be generated for the transistor in the *S*-parameter module. The ADW performance can then be compared to the measured or the harmonic-balance performance or can be compared to the performance listed in the data sheet of the transistor.

The optimum power points, contours and maximum-efficiency lines in the *S*-parameter module are only provided for modeling purposes. The CIL or the Power Matching Network wizards in the Analysis module should be used to design the load networks for power transistors.

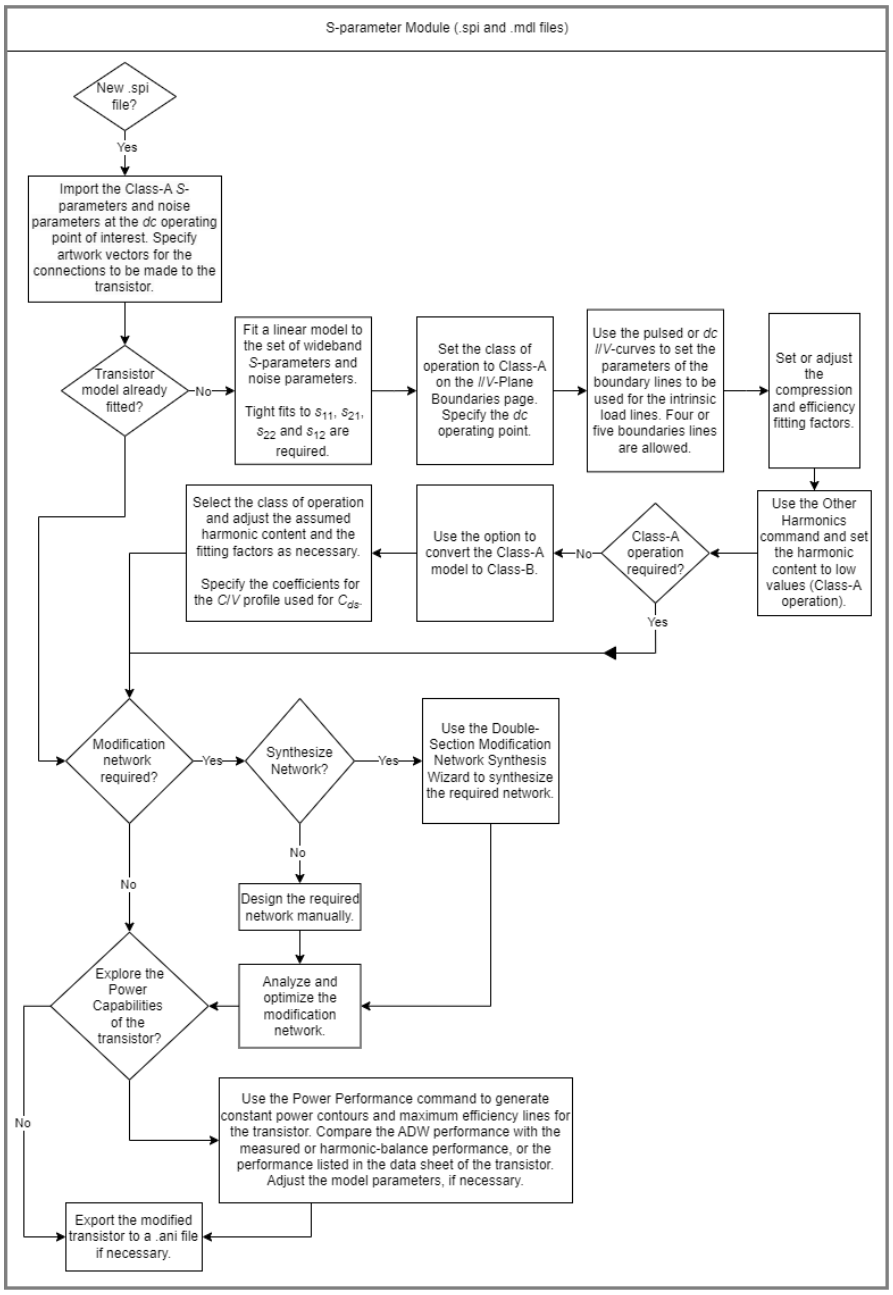

Figure 3. The design flow in the *S*-parameter module.

The ADW load-pull and analysis capabilities are based on clipping theory. (Clipping of the intrinsic load line on the *I*/*V*-plane boundaries defined.) Clipping theory provides a bridge between linear analysis and harmonic-balance analysis.

Clipping theory has been developed to a fully useful point in the ADW: The load terminations presented by a matching network are mapped automatically to the intrinsic reference plane of the transistor by using power parameters and the harmonic content is estimated from continuous mode theory for the assumed class of operation. The classes allowed in the ADW

are Class-A, class-B (including class-AB), class-F, inverse class-F and class-B2. The associated continuous modes are also allowed. Note that the output driving waveform is half-sinusoidal (or approximate half-sinusoidal) current for class-B and class-F, and a half-sinusoidal (or approximate half-sinusoidal) voltage for inverse class-F and class-B2; class B2 stands to inverse class-F as class-B stands to class-F.

Extensive control over the assumed harmonic content is provided in the ADW. Up to five harmonics are considered. Search and optimization features for the assumed harmonic content are also provided to improve the fit of the performance obtained in the ADW with that obtained in a harmonic-balance simulation or in actual measurements (that is, if necessary).

With the intrinsic load terminations calculated and the harmonic content estimated, the intrinsic dynamic load lines can be plotted in the ADW. Four or five boundary lines is used to define boundaries for the dynamic load lines in the intrinsic *I*/*V*-plane. The fifth boundary is used to model the upper-left corner in the transistor knee. Hard clipping on one of the boundaries is assumed. (The power at clipping is the maximum unclipped output power (P_{muc}); note that P_{muc} does not depend on the input match.) A compression curve is used for power levels above or below P_{muc}.

Except for the output capacitance (C_{ds}), the components in the transistor model are assumed to be linear. The default capacitance versus voltage profile used for C_{ds} can be modified by the user.

Continuous-mode theory or the fundamental-frequency load terminations with ideal harmonic terminations for the specified class of operation (FFLL) are used during synthesis. When the designed circuit is analyzed in the ADW, the option to use the actual terminations presented by the matching network (HrLL) is provided. When the HrLL option is used, C_{ds} can be set to be constant or to have the non-linear $C(V)$ profile specified. Fourier analysis is used to calculate the harmonic components of the current in C_{ds}.

Analysis Module Features

Schematic views, artwork views, as well as text views are provided in the ADW Analysis module. Editing features are provided in all the views. If marked for optimization, the selected element value in a schematic view can also be tuned. The optimization bounds set for the value is used to set the tuning range but can be overridden.

Some of the capabilities provided in the ADW analysis module are:

- *S*-parameter analysis.
- Power and efficiency analysis (ADW cascade circuits).
- Stability analysis. This includes loop-gain analysis for an amplifier or oscillator stage.
- Reflection analysis at cascade positions in the circuit.
- Differences in the microstrip models used in the ADW and the harmonic-balance simulator can cause discrepancies in the performance. Instead of using the standard ADW discontinuity models, the parameters of more sophisticated models can be fitted to *S*-parameters obtained in EM simulations, or the discontinuity *S*-parameters can be used directly (recommended). *S*-parameter based models for steps, T-junctions and crosses are provided in the ADW. Note that it always a good idea to export the electrical ADW circuit (not the microstrip circuit) to the harmonic-balance simulator in the initial

stages of a design cycle. The ADW design can then be verified without the complications of the microstrip models. When the EM-based *S*-parameters for the junctions are in place in the ADW, the performance can be restored in the ADW by optimization, and the optimized artwork can then be exported.

- The ADW electrical circuit or the artwork can be exported to Microwave Office™, and the artwork can be exported to Sonnet Software®'s EM. The artwork can also be exported to ADS™ for use in Momentum™ via DXF files. The electrical circuit cannot be exported to ADS™, but an alternative to manually entering the electrical circuit is to use the *S*-parameters for each ADW matching network in ADS for the verification.
- Wizards (CIL, CIR, IIM, IVI, OVI, POW) are provided to set up a variety of impedance-matching problems. These problems are then solved by using the ADW Impedance-Matching Module or the CMA wizard.
- Synthesis (CMA wizard) of distributed T-networks or PI-networks (parallel sections or resonating sections are allowed in the shunt positions of these networks) to control the transmission phase-shift, as well as the match. The synthesis is exact at the passband frequency selected. A systematic search on the design space is done for the best broadband solutions.
- Optimization of passive circuits or designed amplifiers. The intrinsic load terminations can also be optimized.
- The active element in the ADW schematic can be tuned if marked for optimization.

ADW Synthesis Capabilities

1. The microstrip module provided can be used to calculate the dimensions for an electrical line or the electrical characteristics of a microstrip line.

2. Constant-gain (G_T, G_a, G_ω) and constant noise figure circles can be plotted in the CIL and CIR Wizards. The circles can be used as targets when a matching network is designed.

3. Constant-power contours and maximum-efficiency lines for Class-A, Class-B, Class-F, Inverse Class-F and class-B2 amplifier stages can be plotted with the CIL Wizard. Points or circular Smith Chart areas can be set automatically as impedance-matching targets. Smith chart sectors can be set as targets for the second-harmonic and third-harmonic frequencies.

4. Second-harmonic clipping contours (third and higher harmonic voltages assumed to be shorted) can be plotted for the optimum class-B terminations or for any fundamental-frequency termination selected in the power contour section.

5. Extensive impedance-matching capabilities are provided in the Impedance-Matching module.

   At the fundamental frequencies, the targets can be points or circular areas. (The circumference or the inside or outside of a circle can be targeted.) At a harmonic frequency (second and/or third harmonic), the target can be a range of reactance values, or a sector defined by a local origin inside the Smith Chart and two points on the edge of the chart.

A matching problem can be modified by adding fixed elements on the input and/or output side of the networks to be synthesized.

Harmonic trapping is integrated into the synthesis algorithm for non-commensurate matching networks. Different trap frequencies can be specified for the open-ended branches and the shorted branches in the network. The trap frequency for shorted branches must be lower or equal to that for open-ended branches.

Parasitic inductance or capacitance can be added to lumped capacitors or inductors, respectively. The parasitic element can have a fixed value or can be used for harmonic trapping. Different trap frequencies can be specified for the capacitors and the inductors.

When the matching problem was set up with the CIL Synthesis wizard, the intrinsic load lines associated with each solution can be also be viewed in the Matching module.

Lumped-element, commensurate distributed or non-commensurate distributed matching networks can be synthesized. Different lengths are allowed for main-line elements, shorted stubs, and open stubs in ADW commensurate networks.

When non-commensurate networks are synthesized, the characteristic impedances (line widths) are specified by the user and the line lengths are the variables. A systematic search can be done for the optimum main-line characteristic impedance.

When commensurate networks are synthesized, the line lengths are specified by the user and the characteristic impedances (line widths) are the variables. A search can be done for the optimum main-line length. The line lengths can be set for harmonic trapping.

6. Modification networks (lossy sections added to the transistor; feedback or loading sections) can be synthesized to stabilize a transistor, to level the power gain and to improve the input and/or the output VSWRs before matching.

Transistor Modelling Capabilities

Linear bipolar or FET/HEMT transistor models can be fitted to a set of wideband *S*-parameters in the ADW. The standard fitting procedure usually yields a tight fit in the parameters. The boundary constraints on the intrinsic load-line can be obtained from *dc* or pulsed *I*/*V*-curves or estimates can be used. The harmonic content for the different classes of operation is estimated from continuous-mode theory and can be adjusted by the user. The class of operation can be fixed for a model, or mode-switching can be allowed.

The model parameters can be adjusted to improve the fit with the information (gain, power, and optimum terminations) provided in the datasheet or a harmonic-balance simulation. The adjustments can be manual or by using the optimization features provided for this purpose.

Export Capabilities

ADW circuits can be exported in various formats:

- The schematic or artwork can be exported to Microwave Office™ as a basic script (.bas file).
- The schematic or artwork can be exported in HPGL or DXF format. A technology file can also be created for CST Microwave Studio™ when the artwork is exported in DXF format.
- The artwork can be exported as a Sonnet® Software files (*.son).
- The artwork can be exported to Momentum™ in DXF format.

8th April 2024