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High-Efficiency RF Power Amplifier Design Atlas (*H2ID* Complementary Waveform Framework)

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Executive Summary

This document presents a curated atlas of complementary intrinsic current and voltage waveforms derived across the Second-Harmonic Input Distortion (*H2ID*) design space for high-efficiency RF power amplifiers.

The atlas provides a structured mapping between the *H2ID* vector (magnitude and phase) and:

- Complementary normalized intrinsic voltage and current waveforms
- Normalized dynamic load lines
- Achievable waveform efficiency
- Power factor (P_w)
- Conduction angle
- Associated intrinsic harmonic load impedances

This approach enables a waveform-centric design methodology, in which amplifier operation is defined directly in terms of intrinsic voltage and current waveforms, rather than predefined amplifier classes.

Key Observations

- Efficiencies exceeding 90% are achievable for small *H2ID* magnitudes, while efficiencies up to ~87% are achievable at higher distortion levels.
- Classical Class-B and Class-F-like behaviour emerge naturally within the *H2ID* framework.
- Additional high-efficiency operating modes exist beyond classical classes, including inverse Class-F-like operation.
- Class-F-like operation is not supported in certain regions of the *H2ID* plane, where negative harmonic resistance would be required.
- Efficiency is strongly dependent on both the magnitude and phase of the *H2ID* vector.
- Resistive harmonic terminations are required at some operating points to maximize the efficiency.
- Certain regions of the *H2ID* design space inherently yield poor efficiency and should be avoided in practical design.
- In some regions, negative intrinsic source resistance is required, highlighting practical implementation constraints.

- With the same maximum current level targeted, the output power depends on the set of complementary waveforms selected (different power factors).
- The transistor knee lowers the efficiency, as well as the output power. The waveform efficiency is approached at low levels for the maximum current. For the best efficiency, the minimum acceptable output power should be targeted.
- Calculation of the knee effect on the output power and efficiency is simplified when the waveform voltage is close to zero when the waveform current is at its maximum.

This document is intended for:

- RF power amplifier designers
- Microwave engineers
- Academic researchers in waveform engineering

The dataset provided can be used to augment load-pull, harmonic tuning, and waveform engineering workflows, enabling faster and more informed design decisions.

Why This Atlas Is Valuable

Traditional RF power amplifier design relies heavily on:

- Iterative load-pull simulations
- Harmonic tuning experiments
- Trial-and-error optimization

These approaches can be time-consuming and provide limited physical insight into the underlying waveform behaviour.

This atlas introduces a fundamentally different approach:

Waveform-First Design

Instead of searching for optimal impedances, the designer can:

1. Select a desired waveform behaviour (relative efficiency, power factor, effect of variations in *H2ID*, ...) and the associated *H2ID*.
2. Linearise the transistor knee boundary (line segments) and decide on a compromise between power and efficiency. Set the scale factors for the complementary waveforms accordingly. The maximum current associated with the lowest acceptable power will yield the best efficiency.
3. Calculate the required intrinsic harmonic impedances.

4. Use the calculated second harmonic load impedance and create the tuning profile for the *H2ID*. Verify that the *H2ID* targeted is supported by the tuning profile.
5. Map the intrinsic harmonic impedances to the external reference plane.

Key Advantages

- Reduced design time through structured approach
- Direct mapping: *H2ID* → waveforms → efficiency versus power compromise → scale factors → intrinsic impedance → mapping to external reference plane → implementation
- Identification of high-efficiency regions and design avoidance regions
- Insight into non-classical operating modes beyond Class-B and Class-F
- Compatibility with practical limited-harmonic implementations (≤ 3 rd harmonic)
- Insight into the effect of the transistor knee effect on the waveform power and efficiency

This transforms amplifier design from a purely numerical process into a guided, insight-driven methodology.

H2ID Complementary Waveform Method

The approach presented in this atlas is based on the following principles:

H2ID-Defined Current Waveform

The normalized intrinsic output current waveform is determined uniquely by the second-harmonic input distortion (*H2ID*), characterised by its magnitude and phase.

Complementary Voltage Waveform Synthesis

A complementary normalized intrinsic voltage waveform is synthesized to maximize efficiency.

Limited Harmonic Content

The voltage waveforms are constructed using a limited number of harmonics (DC, fundamental, second, and third), ensuring practical realizability.

Hard Clipping

Hard clipping on the transistor knee boundary is assumed. The effect of interaction with the knee (compression) is not considered here.

Constraints Imposed by Transistor Knee

Ideally the *dc* component associated with the scaled voltage waveform should be equal to the actual *dc* voltage. Because of the transistor knee, this is not possible and both the efficiency and the output power will be lower than expected for the complementary waveforms. The higher the maximum for the scaled current waveform, the greater the degradation.

When the current at the point where the dynamic load line touches the knee is close to the peak current, the scale factors for the reductions are only weakly dependent on the complementary waveforms. When the dynamic load line is curved away from the knee above the contact point, the efficiency is determined by the point of contact and not the peak current (Class-F like behaviour). The relevant section of the normalized dynamic load line is shown with the normalized complementary waveforms as an aid to identifying these operating points.

Scale Factors

Without any knee effects, the ideal scale factors for the complementary waveforms are uniquely determined by the maximum device current and the *dc* voltage targeted. When the knee cannot be ignored, the efficiency will be lower than the complementary waveform efficiency. The efficiency increases as the peak waveform current is lowered, while the power decreases. The waveform efficiency is approached at very low currents. The best compromise is to set the maximum waveform current to the level associated with the lowest acceptable output power. The design space can be enlarged by using a range of scale factors.

Intrinsic Harmonic Impedances

The scale factor for the intrinsic load impedances ($Z_{Li1}, Z_{Li2}, Z_{Li3}$) is equal to the ratio of the voltage and the current waveform scale factors (V_{scale}/I_{scale}).

The method reveals that classical amplifier classes represent only a subset of a broader design space.

Overview

Efficiency is a primary constraint in RF power amplifier design, directly affecting thermal performance, reliability, and system cost.

High efficiency requires control of:

- Fundamental-frequency load impedance
- Harmonic load impedances presented to the transistor
- Source impedance presented to the nonlinear input capacitance

In practical devices, nonlinear input capacitances generate harmonic components at the input, modifying the intrinsic input voltage waveform $V_{1i}(t)$. Assuming approximately linear transconductance, the intrinsic output current waveform ($I_{2i}(t)$) follows the shape of the input voltage waveform (rectified and scaled). Changes in input waveform shape are, therefore, directly reflected in the output current, leading to different optimal load conditions.

This work focuses on Second-Harmonic Input Distortion (*H2ID*) and its role in shaping these waveforms.

Rather than defining amplifier operation through fixed harmonic terminations, this atlas adopts a waveform-centric perspective, in which:

- The normalized intrinsic current waveform is defined by the *H2ID* vector
- A complementary normalized voltage waveform is synthesized to maximize efficiency
- The corresponding normalized harmonic impedances are calculated

This approach reveals a rich design space in which:

- Classical Class-B and Class-F behaviour arise naturally
- Additional high-efficiency modes exist beyond classical definitions
- Some regions inherently limit achievable efficiency

The dataset presented here provides a systematic exploration of this design space, enabling practical waveform-based amplifier design. For the results to be practical, the effect of the transistor knee on the efficiency and the output power will also be considered.

Atlas Contents

Each H2ID operating point in this atlas includes:

Waveform Data

- Normalized intrinsic voltage waveform ($V_{2i,H1} = 1.0$)
- Normalized intrinsic current waveform ($I_{2i,H1} = 1.0$)
- Normalized dynamic load line sections relevant to the transistor knee

Metrics

- Waveform efficiency
- Waveform power factor (P_w)
- Current waveform conduction angle

Scaling Parameters

- V_{2i_dc}, V_{2i_max}
- I_{2i_dc}, I_{2i_max}

Harmonic Load Requirements

- Fundamental impedance Z_{Li1}
- Second-harmonic impedance Z_{Li2}
- Third-harmonic impedance Z_{Li3}

Additional Design Information

- Qualitative classification (e.g., Class-F-like, inverse Class-F-like)
- Indicators of practical constraints (e.g., negative intrinsic source resistance requirements)

Practical Use of This Atlas

The data provided in this document can be used to:

- Pre-select high-efficiency operating regions before designing a power amplifier
- Define target harmonic impedances for load-pull or matching design
- Guide waveform engineering using limited harmonic control
- Identify regions of the design space that should be avoided

The atlas is intended to complement, not replace:

- Circuit simulation
- Load-pull measurements
- Harmonic tuning

It provides structured insight that significantly reduces design iteration effort.

Device Limits and Constraints

The maximum drain current and drain voltage of the transistor to be used and the boundaries associated with the transistor I/V -curves must be considered when the normalized complementary waveforms are scaled.

When the knee can be ignored, the waveform should be scaled by the factor

$$V_{scale} = V_{dcA}/V_{dcW} \quad (1)$$

to maximize the efficiency. V_{dcW} is the dc voltage associated with the normalized voltage waveform and V_{dcA} is the actual dc voltage.

When the knee cannot be ignored and the actual dc voltage is fixed, only the ac part of the intrinsic voltage waveform ($V_W(\theta)$) is scaled. The scaled voltage waveform ($V_A(\theta)$) is then defined by

$$V_A(\theta) = (V_W(\theta) - V_{dcW}) \times V_{scale} + V_{dcA} \quad (2)$$

The scaled current waveform ($I_A(\theta)$) is defined by

$$I_A(\theta) = I_W(\theta) \times I_{scale} \quad (3)$$

where $I_W(\theta)$ is the normalized intrinsic current waveform.

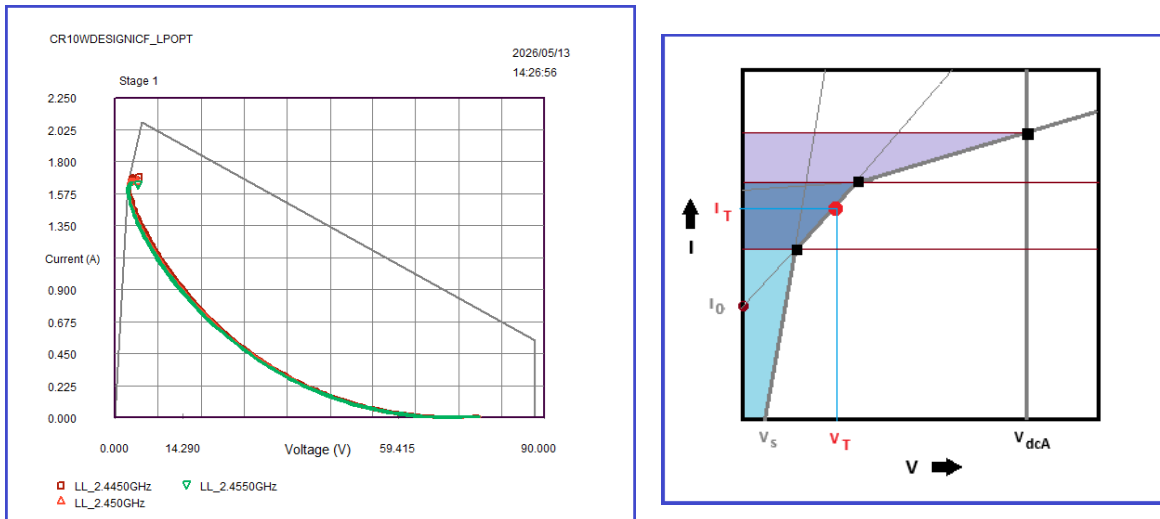


Figure 1. The I/V -curve boundaries were linearized in the Class-F load-pull example shown on the left. Three segments were used to model the knee in the RHS plot.

The boundary condition imposed by the knee on the scaled voltage and current waveforms is

$$V_A(\theta) \geq [I_A(\theta) - I_{0B}] \times R_{sB} \quad (4)$$

R_{sB} is the resistance associated with the active boundary line (see Figure 1) and I_{0B} is the intersect of this line with the vertical axis. It follows from (4) that

$$[(I_A(\theta) - I_{0B}) \times R_{sB}] / V_A(\theta) \leq 1.0 \quad (5)$$

For maximum efficiency, V_{scale} should be the maximum allowed by (5). The equality in (5) will apply at the point(s) where the dynamic load line touches the knee boundary ((V_{TK}, I_T)). The required scale factor can also be determined graphically by plotting the boundaries and the scaled dynamic load line, with V_{scale} tuned.

With the scale factors for the current and the voltage known, the scale factor for the normalized intrinsic impedances is also known:

$$Z_{scale} = V_{scale} / I_{scale} \quad (6)$$

...

Based on the above, the following procedure can be followed to decide on the scaling factors to be used:

1. **Linearize** the **boundaries** associated with the I/V -curves of the transistor of interest (see Figure 1).
2. Decide on the complementary set of waveforms to be used (**H2ID operating point**). P_w (see equation (14)) is a figure of merit for each H2ID operating point.
3. Use the linearized knee boundaries and the complementary waveform data provided in the H2ID dataset to find the optimum scale factors for the normalized intrinsic voltage waveform at different maximum current levels (I_{maxT}). Then use equations (21), (22) and (23) to calculate the **power and efficiency** at the selected current levels. For reasonable values of efficiency, the power will decrease as the efficiency increases.
4. Decide on a point or points with acceptable power and efficiency and use the associated scale factors to calculate the intrinsic load terminations.

When the normalized intrinsic voltage is close zero when the normalized intrinsic current is a maximum, the optimum voltage scale factor can be approximated by:

$$V_{scale} = (V_{dCA} - R_{sB} \times I_{maxT}) / V_{dcW} \quad (24)$$

...

Typical Workflow

1. Select some of the operating points based on the performance required, the figure of merit (P_w), the expected behaviour with increasing second-harmonic input distortion and any constraints on the **H2ID vectors**.
2. **Scale** the voltage and current associated with each selected operating point by following the procedure outline above and then scale the intrinsic load impedances accordingly.
3. If a model is available, use the second harmonic intrinsic load termination associated with each H2ID vector to generate the **tuning profile** for the external source reflection coefficient (H2ID versus source reflection coefficient angle – refer to Appendix A). If the H2ID vector is not supported in the profile, select a vector which is supported and rescale the voltage and current for the new operating point.
4. Map the intrinsic impedances to the **external reference plane**.
5. With the required load tuners or load matching network in place, match the input of the transistor at the fundamental frequency (add resistance for stability, if required) and set the second-harmonic source termination to the corresponding reflection coefficient in the tuning profile. If no second-harmonic tuning profile was generated, tune the **external second-harmonic source impedance** to optimize the performance, or to minimize the difference between the H2ID vector calculated and the H2ID vector targeted.
6. Tune the complete circuit for optimum performance.
7. Establish the variations allowed from the optimum terminations for acceptable performance.

Note that H2ID is directly dependent on the intrinsic source impedance (Z_{Si}) presented to the nonlinear input capacitor (Thevenin impedance). Z_{Si} depends on the external source impedance, as well as the intrinsic second-harmonic load impedance and internal feedback and loading in the transistor. The mapping of the external source impedance to the intrinsic source impedance limits the useable H2ID operating points (harmonic injection could be considered to solve this).

A model of the transistor (or at least the parasitic components on the outside side of the transistor) is required to map the intrinsic load impedances to the external reference plane. In the Ampsa Amplifier Design Wizard (Ampsa ADW), a small-signal model is fitted to a set of wideband S-parameters, after which the power parameters are calculated and used for the mapping. Assuming linearity, the mapping is exact (feedback and loading included) - In practice, the correlation with harmonic-balance results is usually excellent.

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Harmonic Content of *H2ID* Current Waveforms

The number of harmonics in the complementary voltage waveforms were limited to three. Intrinsic shorts are required at the higher harmonics to prevent degradation of the performance. The matching networks designed are, however, unlikely to provide exact shorts at these harmonics and the number of significant harmonics in the *H2ID* current waveform and the actual terminations presented at these harmonics are, therefore, also important.

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Ampsa H2ID Atlas – Version 2C

The maximum waveform efficiency obtainable (η ; %) and the Complementary Waveform Power Factor (P_w) as a function of the H2ID magnitude and phase.

H2IDang	180°	180°	190°	190°	200°	200°	210°	210°	225°	225°	240°	240°
H2IDmag	η	P_w	η	P_w	η	P_w	η	P_w	η	P_w	η	P_w
0.01	90.3	0.5806	90.2	0.5790	90.2	0.5795	90.0	0.5779	90.3	0.5788	90.1	0.5759
0.05	88.7	0.5948	88.7	0.5944	88.8	0.5933	89.0	0.5915	89.3	0.5877	89.7	0.5836
0.10	86.4	0.6141	86.5	0.6129	86.7	0.6095	87.1	0.6044	87.9	0.5951	89.0	0.5858
0.20	80.5	0.6529	81.6	0.6506	82.0	0.6326	82.9	0.6142	84.8	0.5903	87.6	0.5747
0.30	71.3	0.6592	74.4	0.6418	78.4	0.6321	79.2	0.5978	81.1	0.5589	85.5	0.5434
0.36	66.8	0.6358	87.4	0.7631	83.9	0.6770	78.0	0.5845	78.5	0.5321	83.6	0.5174
0.40	64.2	0.6125	67.1	0.5848	87.0	0.6974	82.9	0.6151	76.7	0.5126	82.1	0.4990
0.50	59.7	0.5581	63.3	0.5376	68.6	0.5339	82.3	0.5906	78.1	0.5020	77.6	0.4512

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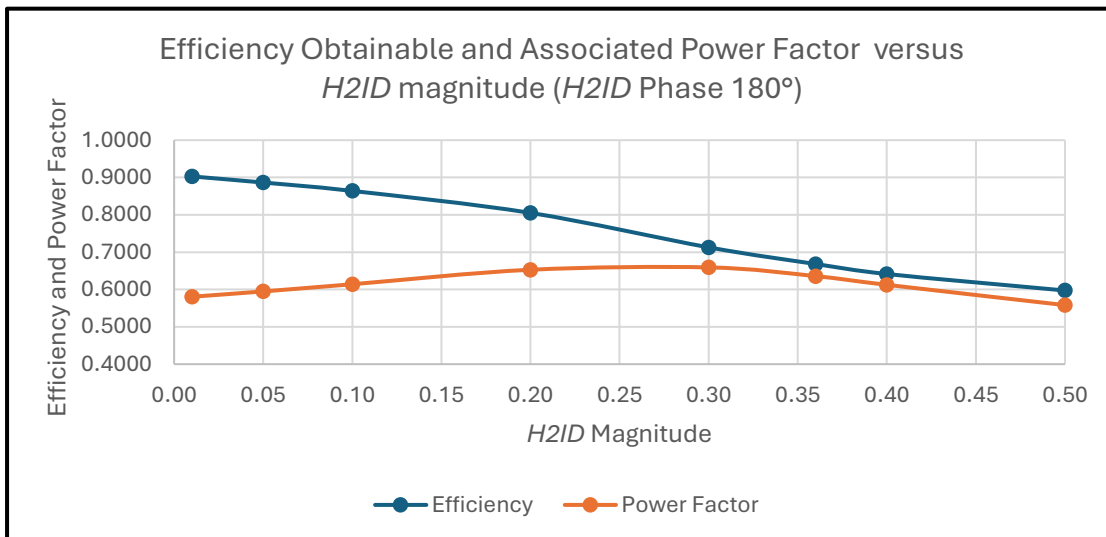
	[90.0; 100]
	[85; 90)
	[80; 85)
	[75; 80)
	[70; 75)
	[65; 70)
	[60; 65)
	[55; 60)
	[50; 55)

The maximum waveform efficiency obtainable (%) and the current waveform conduction angle (degrees) as a function of the *H2ID* magnitude and phase.

<i>H2IDpha</i>	180°	180°	190°	190°	200°	200°	210°	210°	225°	225°	240°	240°
<i>H2IDmag</i>	η	CA	η	CA	η	CA	η	CA	η	CA	η	CA
0.01	90.29	181.1	90.19	181.1	90.18	181.1	90.00	181.0	90.29	180.8	90.06	180.6
0.05	88.65	185.7	88.69	185.6	88.79	185.4	88.96	185.0	89.27	184.1	89.73	182.9
0.10	86.40	191.3	86.48	191.1	86.72	190.6	87.09	189.9	87.89	188.2	88.95	185.9
0.20	80.52	201.5	81.55	201.2	82.04	200.6	82.90	199.4	84.80	196.7	87.60	192.6
0.30	71.29	210.1	74.38	209.9	78.44	209.3	79.20	208.2	81.08	205.4	85.53	200.7
0.36	66.83	215.5	87.37	214.3	83.92	213.8	77.99	212.8	78.52	210.3	83.57	205.9
0.40	64.15	217.2	67.10	217.0	86.99	216.5	82.86	215.6	76.71	213.4	82.05	209.4
0.50	59.73	222.9	63.32	222.8	68.61	222.5	82.25	221.8	78.08	220.3	77.60	217.5

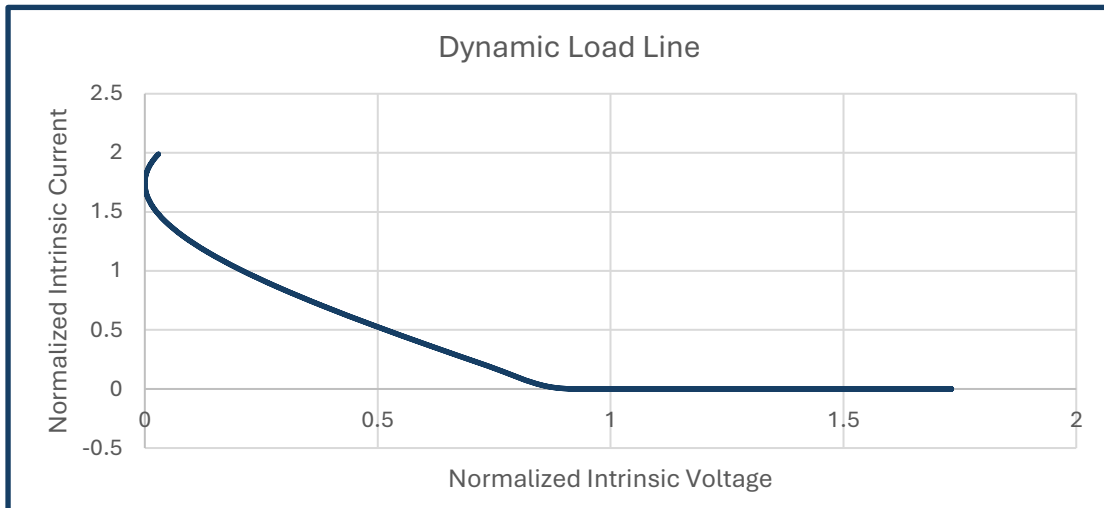
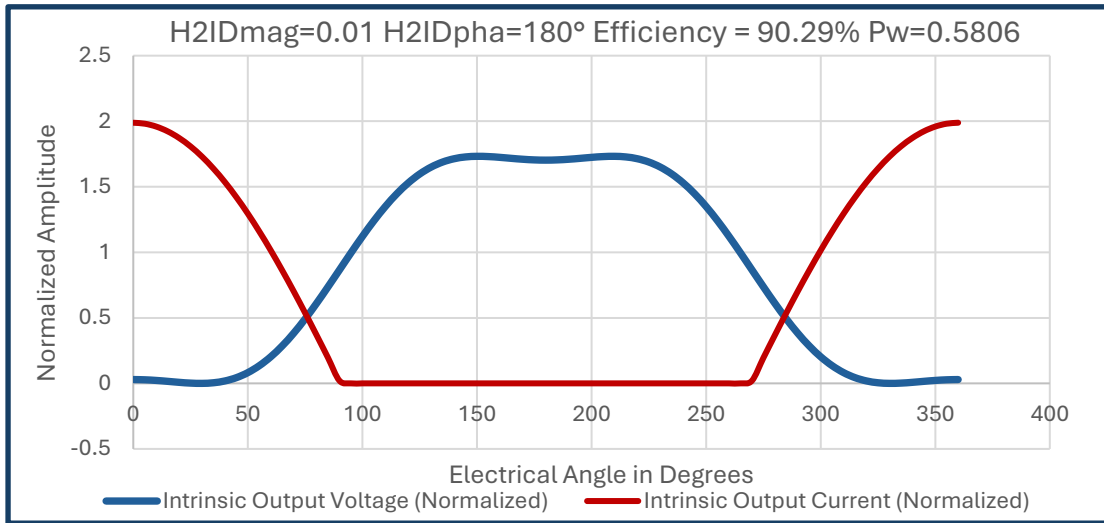
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Maximum Efficiency Obtainable and Associated Power Factor (P_w) versus *H2ID* Magnitude for different *H2ID* Phase Angles



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Selected High Efficiency H2ID Complementary Waveforms

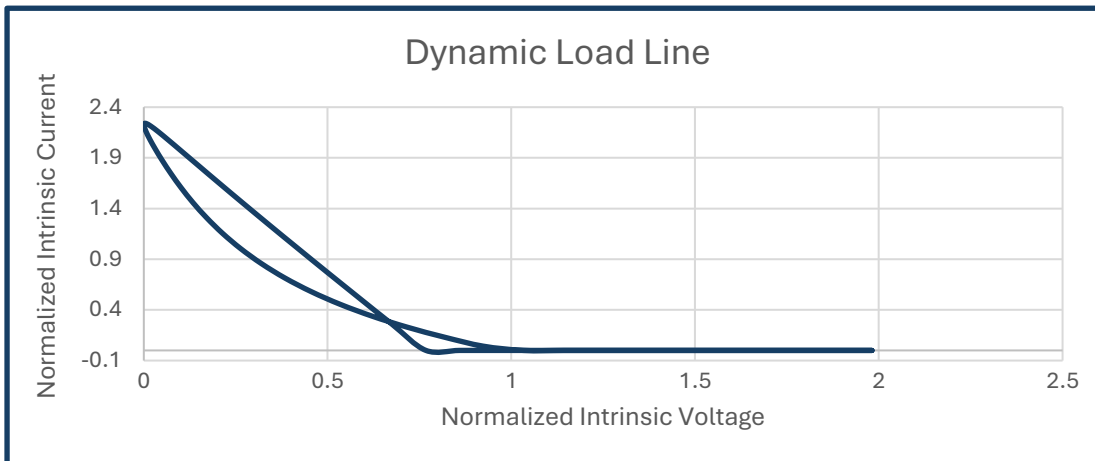
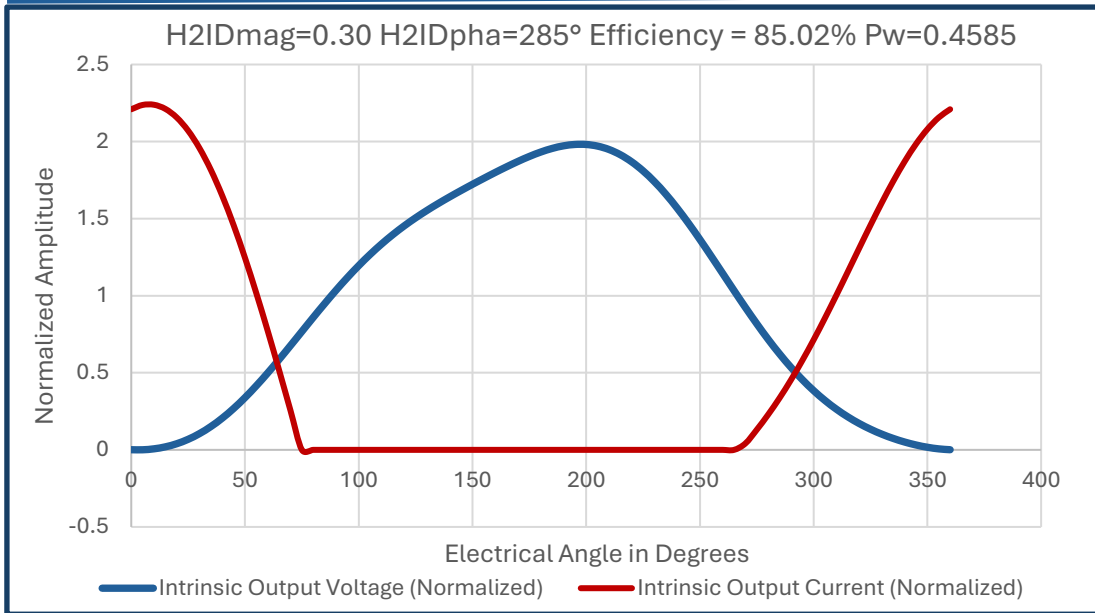


Scaling Parameters

Parameter	Value	Parameter	Value
V_{dc}	0.8661	I_{dc}	0.6394
V_{max}	1.7322	I_{max}	1.9884
V_{2i_H1}	1.0000	I_{2i_H1}	1.0000
P_w	0.5806		

Harmonic Load Requirements

Harmonic	Impedance
Fundamental (Z_{Li1})	1.0000 + j0.0000
2nd Harmonic (Z_{Li2})	0.0000 + j0.0000
3rd Harmonic (Z_{Li3})	21.2539 + j0.0000



Scaling Parameters

Parameter	Value	Parameter	Value
V_{dc}	0.9728	I_{dc}	0.6046
V_{max}	1.9824	I_{max}	2.2417
V_{2i_H1}	1.0000	I_{2i_H1}	1.0000
P_w	0.4585		

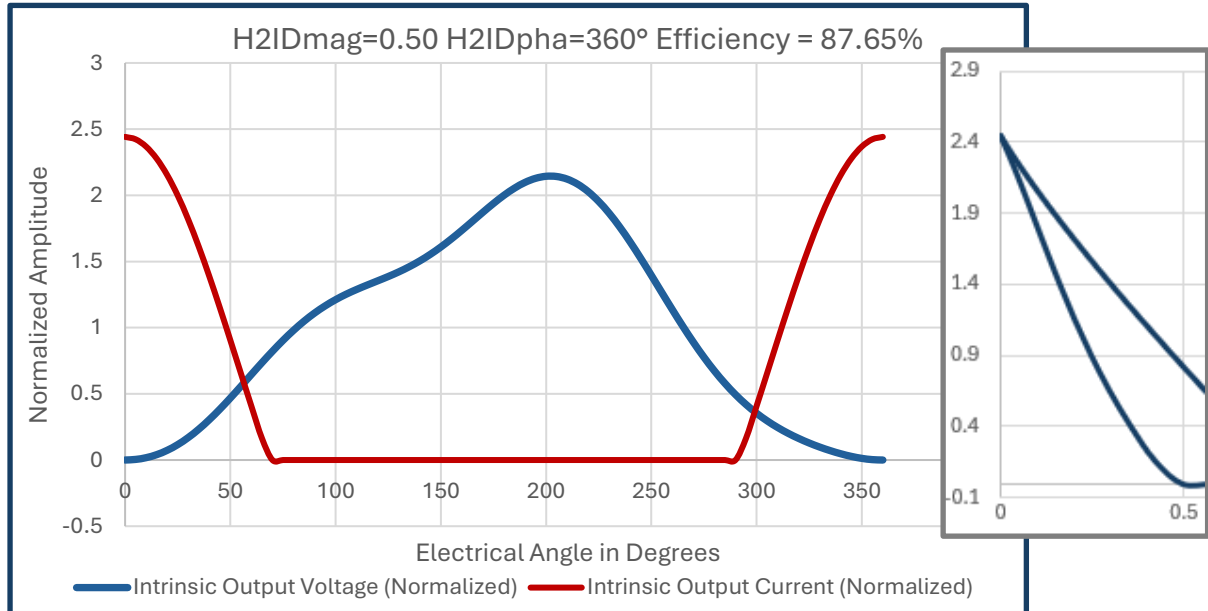
Harmonic Load Requirements

Harmonic	Impedance
Fundamental (Z_{Li1})	1.0000 + j0.0000
2nd Harmonic (Z_{Li2})	0.0000 + j0.1228
3rd Harmonic (Z_{Li3})	0.0000 - j0.4281

H2ID Operating Point (0.50; 360°; 87.65%; 0.4095)

Magnitude: 0.50 Phase: 360° Efficiency: 87.65% Power Factor: 0.4095

Intrinsic Waveforms



Design Classification

High efficiency. Moderate third-harmonic impedance. Class-B-like waveforms, with the voltage waveform triangular. Conduction angle 137.1°.

Scaling Parameters

Parameter	Value	Parameter	Value
V_{dc}	1.0000	I_{dc}	0.5704
V_{max}	2.1452	I_{max}	2.4416
V_{2i_H1}	1.0000	I_{2i_H1}	1.0000

Harmonic Load Requirements

Harmonic	Impedance
Fundamental (Z_{Li1})	1.0000 + $j0.0000$
2 nd Harmonic (Z_{Li2})	0.0000 + $j0.2586$
3 rd Harmonic (Z_{Li3})	0.0000 - $j0.4040$

Appendix B

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