Fitting Ampsa ADW Transistor Models

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Overview

Transistor *S*-parameters can be used to calculate and control the gain and the impedances of a linear amplifier but cannot be used to calculate or control the power. Non-linear transistor models and harmonic-balance or time-domain simulators are usually used for this purpose. Linear amplifiers are, however, generally well behaved when they are not driven into deep compression. It should, therefore, be possible to calculate and control the power on a linear basis. This capability is provided in the Ampsa Amplifier Design Wizard and is discussed below. The accuracy of the ADW approach is good enough for synthesis purposes. With some fine-tuning to the ADW transistor models, a tight fit can usually be obtained to a harmonic-balance simulation, even under moderate compression. Compared to the effort involved in fitting an accurate non-linear model, the effort required to fit an ADW transistor model is insignificant.

Introduction

S-parameters are used to characterize transistors in the ADW. To estimate the power extracted from a transistor and to control its power performance, an ADW small-signal model must be fitted to each transistor. A set of linear power parameters [1] is then calculated for each transistor by using the model fitted. The power parameters are used to map the intrinsic voltages and the intrinsic output current of the transistor to the external voltages. This allows calculating the intrinsic voltages and current for any load termination. The intrinsic load impedance presented to the transistor can be calculated from the intrinsic output voltage and current. The maximum power for a given intrinsic load termination is limited by constraints on the intrinsic output voltage and current. The *dc* or pulsed *I*/*V*-curves of a transistor can be used to set boundaries for the intrinsic dynamic load line. Four of five boundary lines can currently be used to define the allowable load line area in the ADW (see Figure 1).

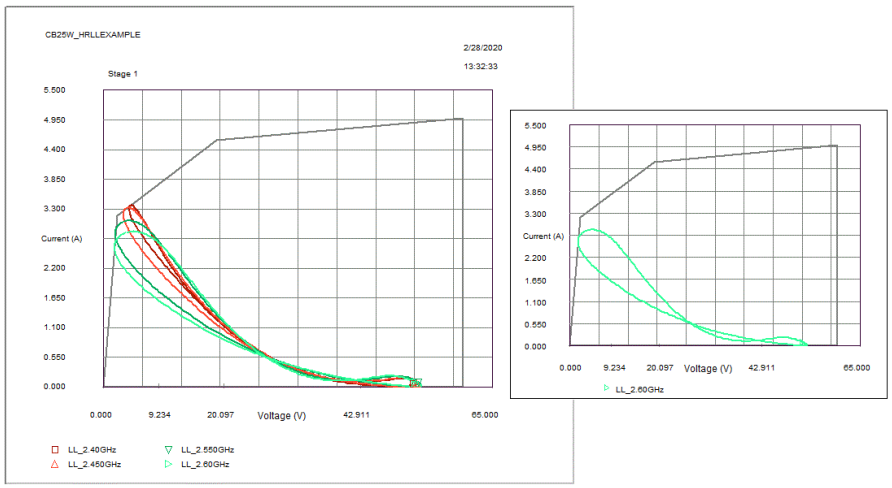


Figure 1. An example of the *I*/*V*-plane boundary lines set for a transistor (25W Cree GaN transistor).

The fundamental-frequency and the harmonic components of the output intrinsic driving waveform (current in a class-B stage, …) and the intrinsic load impedances (or admittances) determine the output intrinsic response waveform (voltage in a class-B stage, …), to first order.

Harmonic components which are not present in the driving waveform can also be generated in the response waveform (consider the third-harmonic voltage in class-F operation). The components generated can distort the driving waveform via the associated intrinsic load impedances (or admittances) if these impedances or admittances are not ideal (open or short). The behaviour of the intrinsic dynamic load line is, therefore, determined by the harmonic content of the driving waveform, the harmonic content generated in the response waveform and the intrinsic load terminations.

In the ADW, the class of operation (class-A, class-B, class-F, inverse class-F or class-B2; class-B2 stands to inverse class-F as class-B/J stands to class-F) is fixed for a specific transistor model. Two analysis modes are provided for each class. In the default mode (FFLL), the harmonic voltages and currents, as well as the harmonic terminations, are assumed to be the ideal for the assumed class of operation. The circuit behaviour is, therefore, fully determined by the class selected and the fundamental-frequency terminations. In the other mode (HFLL), the harmonic content can be controlled, and the actual intrinsic harmonic terminations presented by the circuit to the transistor are used. Scale factors for the HFLL harmonic content can be set when the transistor model is fitted. The scale factors can be adjusted or can be optimized to improve the correlation with measurements or a harmonic-balance simulation of the circuit.

The frequencies at which the circuit will be analyzed are important when the HFLL analysis mode is used. If a harmonic frequency is not defined in the ADW frequency list (Project | Frequencies menu command), the harmonic load termination at that frequency will be assumed to be the ideal for the base class targeted. The actual intrinsic load impedance at that frequency will then not be used.

The FFLL analysis assumes base class behaviour, while continuous modes are also covered by the HFLL analysis. (For class-J stages, set the base class to class-B and the analysis mode to HFLL.) The analysis mode can be set by using the Project | Options menu command in the ADW Analysis Module (refer to Figure 2). (Unselect the Ignore Actual Harmonic Terminations option to set the HFLL mode.)

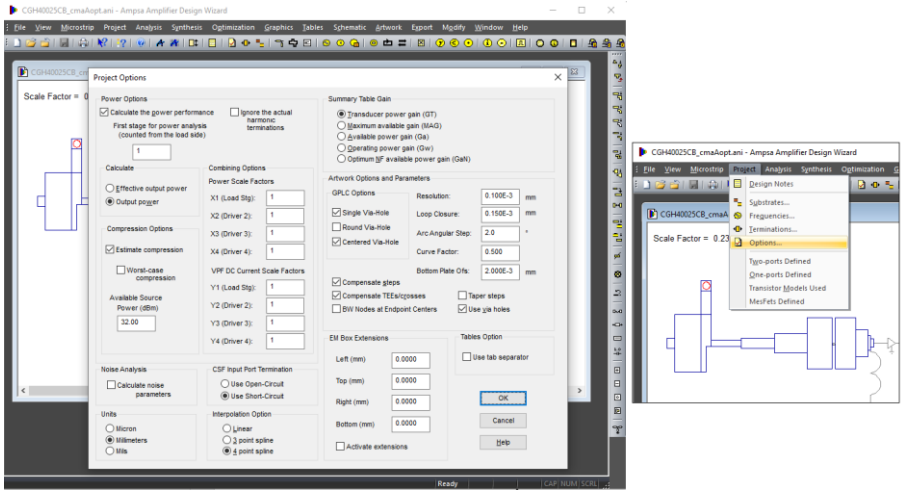


Figure 2. Use the Project | Options menu command and unselect the Ignore Actual Harmonic Terminations option to set the harmonic-frequency analysis mode (HFLL).

Linear behaviour is assumed for the voltage and current components when the intrinsic dynamic load line is inside the boundaries defined. A compression curve [2] is used to model

the behaviour when the load-line is pushed into a boundary. The compression factor set in the model determines whether the compression will be soft or hard. Different compression factors can be set for the two analysis modes.

No compensation has been implemented yet for changes in s_{11} caused by deep compression. Adjustments to the ADW circuit designed can be made in the harmonic-balance simulator to compensate for any discrepancies caused by this.

The FFLL mode is currently used when power contours are generated in the ADW. (Power contours can be generated for any of the base classes.) Ideal harmonic content and harmonic terminations are, therefore, assumed. When continuous-mode operation is required, use one of the continuous class synthesis options provided in the CIL wizard. (Select to control the intrinsic load line directly instead of selecting the power contours option.) Second-harmonic clipping contours [3] can also be generated in the ADW. Note that these contours are not limited to current clipping load lines, as is commonly misunderstood.

A wizard is provided to fit transistor models in the ADW. This wizard is launched when the Data | Transistor Model menu command is used when a ".spi" document (ADW *S*-parameter file) has been created or has been opened (refer to Figure 3). The same wizard can also be launched when an ADW circuit (".ani" document), in which the transistor model of interest is used, has been opened. The Project | Transistor Models Used menu command can then be used to launch the wizard (see the RHS of Figure 3). This command is generally only used to view or adjust a transistor model fitted previously.

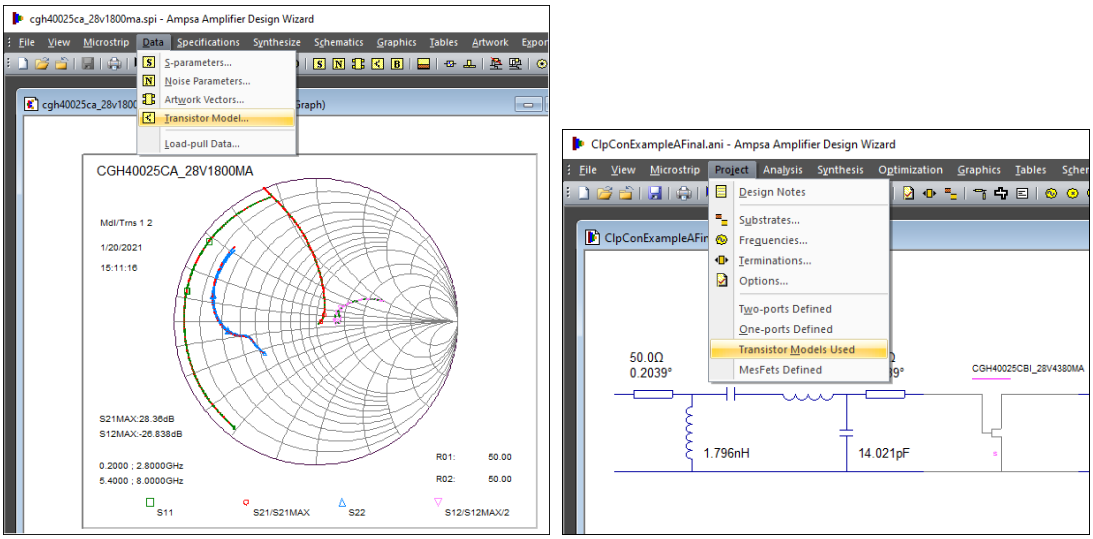
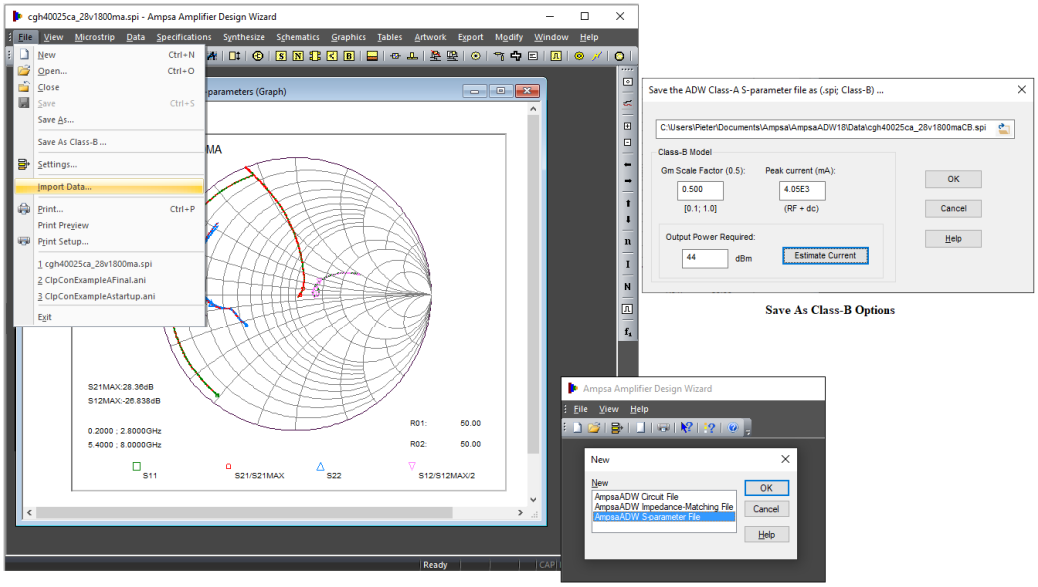


Figure 3. The menu commands used to launch the wizard for fitting an ADW transistor model.

Fitting ADW Transistor Models

The ADW cycle to fit a model to a set of *S*-parameters is started by opening a new ".spi" document. The *S*-parameter data can be entered manually by using the Data | *S*-parameters menu command or automatically by using the File | Import Data menu command (see Figure 4). The *S*-parameters imported are usually class-A parameters. When the model has been fitted,

the Save As Class-B menu command shown in Figure 4 can be used to convert the model for class-B operation.



Save As Class-B Options

Figure 4. When a new ".spi" document has been opened, *S*-parameter data can be imported into the document by using the Import Data menu command. A class-A model can be converted to class-B by using the Save As Class-B command.

The peak current allowed for class-B operation is higher than that for class-A (more power can be extracted because of the higher efficiency). The peak current required to extract the maximum power expected from a transistor can be calculated by using the Estimate Current command shown in Figure 4.

The transconductance for an ideal class-B stage should be half of that of an equivalent class-A stage. Most class-B stages are, however, class-AB stages and the transconductance in such a case can be set to be the small-signal transconductance of the class-AB stage. If a model is fitted to the class-AB parameters of interest, the G_m scale factor in Figure 4 should be set to 1.0. When a single-stage amplifier with the transistor of interest has been designed, the transconductance can be adjusted for good agreement with a harmonic-balance simulation of the amplifier stage designed, if necessary.

Class-A models can be fitted for a range of *dc* current levels to verify that the variations in the transconductance, and the capacitances and inductances, are reasonable.

The pages provided by the FET | HEMT wizard are shown in Figures 5 through 9. Note the Initialize and Optimize commands in Figure 5. The sequence for fitting a model is usually to initialize the intrinsic components by restricting the bandwidth for the fit to lower frequencies (the effect of the extrinsic components should then still be small) and then to optimize the model over the whole frequency range of interest. Start by first fitting the *Y*-parameters and switch to fitting the *S*-parameters when a reasonable fit has been obtained.

Components with zero values are not optimized in the ADW and small values should be specified for the expected extrinsic components before optimization over the whole frequency range. Note that lumped components, as well as transmission lines are allowed in the extrinsic network.

Constraints should be set on all the variables to be optimized. If a variable is constrained and a good fit has not been obtained yet, the constraints should be extended.

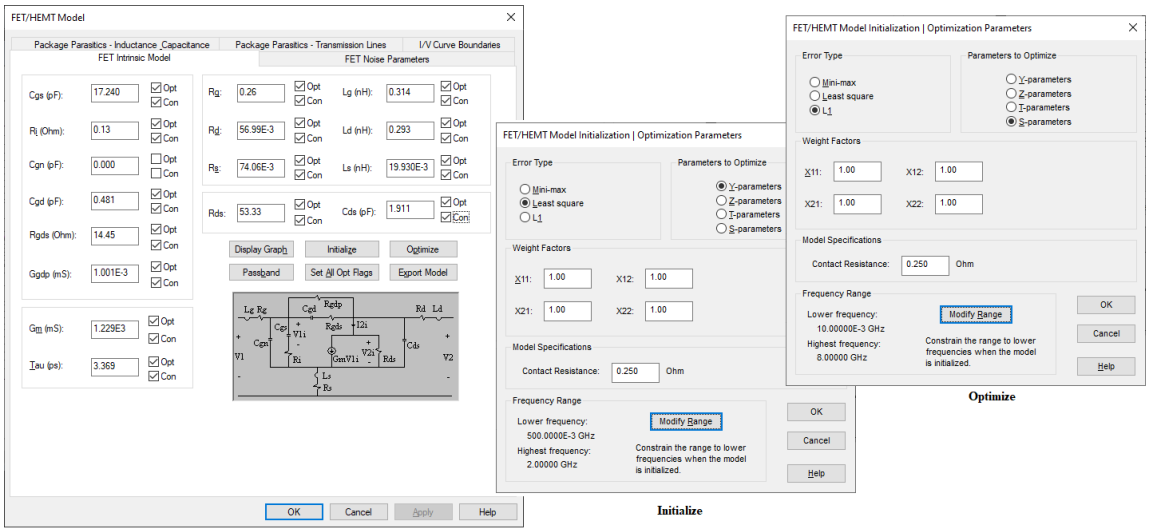


Figure 5. The intrinsic parameters of the transistor are listed on the first page of the wizard. The Initialize command is used to initialize the intrinsic components in the model. The Optimize command is used to obtain a tight fit to the measured parameters.

If noise parameters are available, the noise parameters can be included in the optimization. The frequency range over which the noise parameters are fitted can be different from that for the *S*-parameter fitting. Fukui, Pucel and Pospieszalski noise models are supported in the ADW (see Figure 8).

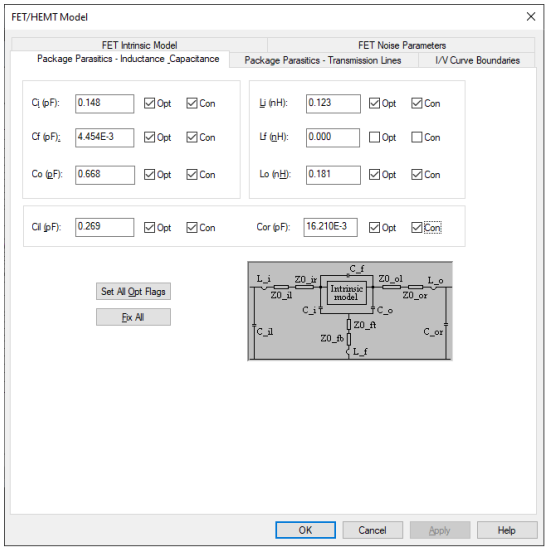


Figure 6. The inductances and capacitances in the extrinsic section of the transistor model are listed here.

The class of operation, the *I*/*V*-plane boundary lines and the *dc* operating point must be specified on the wizard page shown in Figure 9. The class of operation specified is that of the base class. When the performance with the actual harmonic terminations is considered (HFLL), continuous mode operation will also be detected. (The potentially negative effect of a reactive fundamental-frequency intrinsic load termination can be partially or fully cancelled by a compensating second-harmonic intrinsic termination under continuous-mode operation. The

performance can also be degraded by harmonic terminations which consume some of the available swing in the intrinsic voltage or current.)

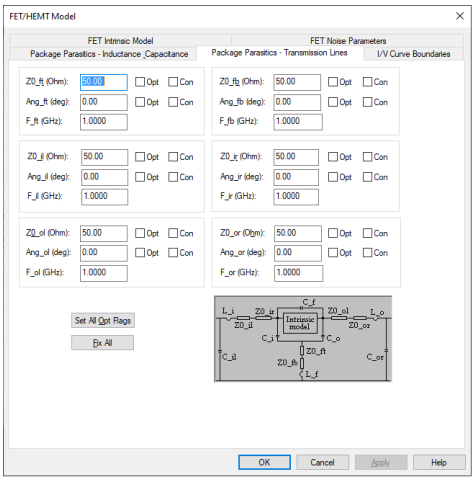


Figure 7. The parameters of the transmission lines in the extrinsic section of the transistor model are listed here.

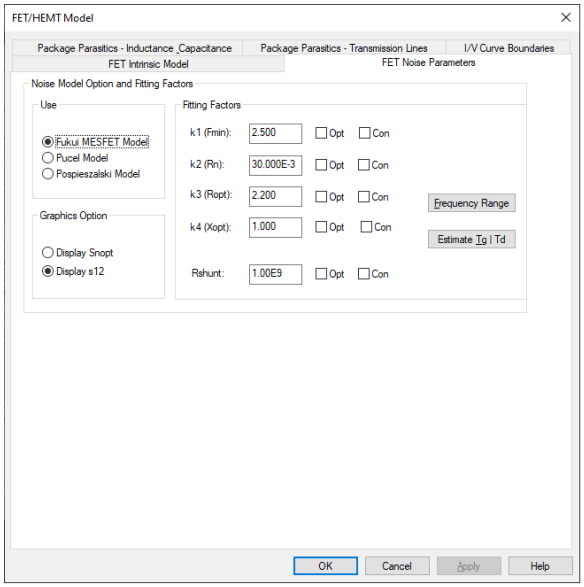


Figure 8. A noise model can be fitted to a transistor too. The parameters of the model can be specified here.

The intrinsic output driving waveform is an exact or approximate half-sinusoidal current when the class of operation is class-B, class-J, or class-F. In inverse class-F mode or class-B2 mode, the intrinsic output driving waveform is an exact or approximate half-sinusoidal voltage.

Gain compression and efficiency fitting factors, as well as a scale factor for the third-harmonic content in the response waveform can also be specified on *I*/*V*-plane Boundaries page. The Limit Output Driving Waveform to Three Harmonics option is usually the better option. (A perfect half-sinusoid can only be obtained at relatively low frequencies.) This option is ignored in class-A stages.

A gain compression factor is the difference between the saturated power level (P_{sat}) and the power level when the dynamic load-line just touches one of the boundary lines (P_{muc}; maximum unclipped power). Gain compression factors must be specified for harmonic-frequency intrinsic load lines (HFLL), as well as fundamental-frequency load lines (FFLL). The

compression factors can initially be set to 3 dB for class-A, Class-B, and class-F operation, and to 0.5 dB for inverse class-F and class-B2 operation. The compression factors can be adjusted for better correlation with a harmonic-balance simulation when a single-stage amplifier has been designed with the transistor of interest.

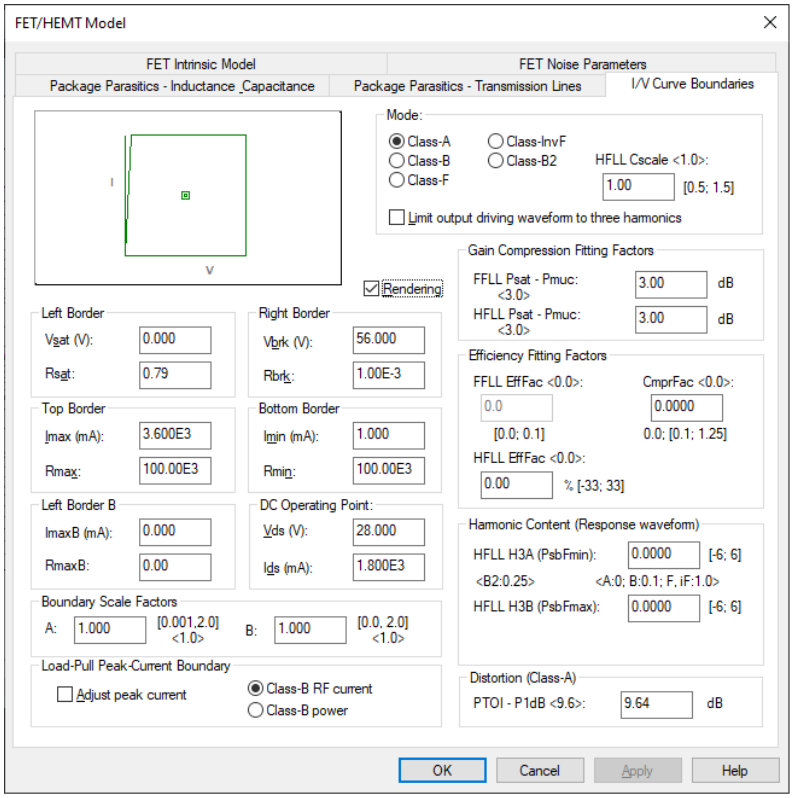


Figure 9. The class of operation, the *I*/*V*-plane boundary lines and the *dc* operating point must be specified on this wizard page. Gain compression and efficiency fitting factors, as well as scale factors for the harmonic content can also be specified here.

The efficiency fitting factors can be set to zero initially.

C_{mprFac} in Figure 9 is used to improve the fit with the efficiency calculated in a harmonic-balance simulator when the output power exceeds the maximum unclipped level (P_{muc}). If this fitting factor is set to 1.0, the *dc* current is assumed to increase linearly with increasing output power and the efficiency will, therefore, remain constant when the output power is more than P_{muc} (stage driven into compression). Below this level, the fitting factor used is 0.5. When C_{mprFac} is set to 0.5, the efficiency will increase with the square root of the ratio of the compressed power and the maximum unclipped power. (The compressed power will eventually saturate.) C_{mprFac} can be set to zero or can be in the range [0.25, 1.25]. If it is set to zero, a factor 0.5 will be used for class-A stages, while 1.0 will be used for class-B, class-B2, class-F and inverse class-F stages.

H_{FLL_EffFac} is associated with the harmonic load-line option (actual fundamental-frequency and harmonic-frequency intrinsic load terminations considered). It is used to adjust the *dc* current estimated. When the current waveform is the driving waveform (class-B, class-J, and class-F) and it is not distorted by the harmonic components generated in the response waveform, the *dc* current in the ADW is assumed to be the *dc* component of the assumed intrinsic output current waveform. In all other cases, the *dc* current is set to force the minimum of the instantaneous intrinsic output current associated with P_{muc} to zero. (That is, the minimum instantaneous

current when a clipping boundary has been reached is set to zero.) The intrinsic output current calculated in a harmonic-balance simulation may, however, ripple around zero instead of being zero or larger. (Using more harmonics may resolve this.) The efficiency is improved by this effect. Higher harmonics may also shape the waveforms to yield higher efficiencies. H_{FLL_EffFac} is the percentage by which the *dc* current calculated in the ADW will be decreased to allow for the ripple and wave shaping effects. Negative values can be used to increase the *dc* current. Values up to 33.3% of the *dc* current calculated are allowed.

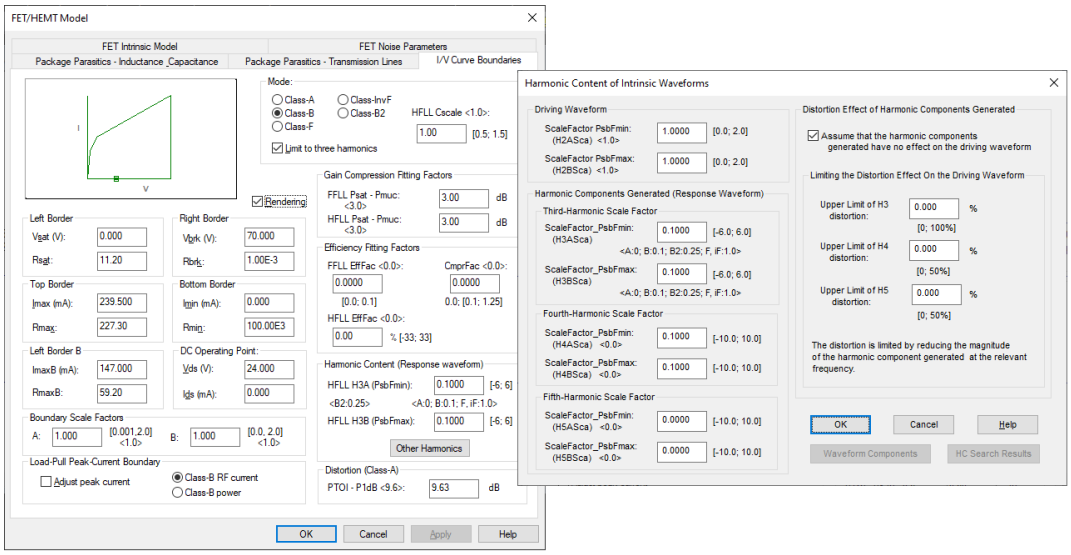


Figure 10. The *I*/*V*-plane boundaries page provided in the Analysis Module. Class-B operation is assumed.

Negative values for H_{FLL_EffFac} can also be used to model the effect of class-AB operation on the efficiency. Alternatively, H_{FLL_EffFac} can be set to zero and the quiescent current (*dc* operating point current) can be specified. The Pedro approach to estimating the total *dc* current [5] is followed in the ADW when the analysis is done with the actual harmonic terminations.

F_{FLL_EffFac} is used to improve the match between the efficiency calculated in the ADW and that obtained in a harmonic-balance simulation when the harmonic terminations are assumed to be the ideal for the base class targeted. The efficiency calculated is reduced when the maximum unclipped current is less than the current associated with maximum power. This factor must be in the range [0.0, 0.1] and its default value is zero. Small values (say, 0.03 or less) are usually required. When the value of this fitting factor is set to zero, it has no effect on the ADW efficiency calculations. This factor is not used when the actual harmonic terminations are used. It is also not used in Class-A stages.

The third harmonic content scale factors in Figure 9 should be 0.0 for ideal class-A and class-B operation. Note that different harmonic content scale factors can be used at the lowest and the highest passband frequencies. Linear interpolation is used in between. Start by assuming the scale factors to be constant over frequency.

If the wizard is opened in the ADW Analysis Module, the scale factors used for the other harmonics can also be modified (see Figure 10). The second harmonic content of the driving waveform, and the third, fourth and fifth harmonics of the response waveform can be modified. (Note that the non-linear behaviour of C_{gs} can create an out-of-phase second harmonic in the gate waveform [4] which will lower the second harmonic content in the output driving

waveform when the output driving waveform is the current.) Select the Other Harmonics command shown in Figure 10 to modify the harmonic content.

Any harmonic generated in the response waveform will distort the driving waveform via the relevant harmonic impedance or admittance. If the ideal harmonic impedances or admittances for the mode of operation are in place, the driving waveform will not be distorted. The option to ignore these effects, as well as options to limit these effects are provided (refer to Figure 10).

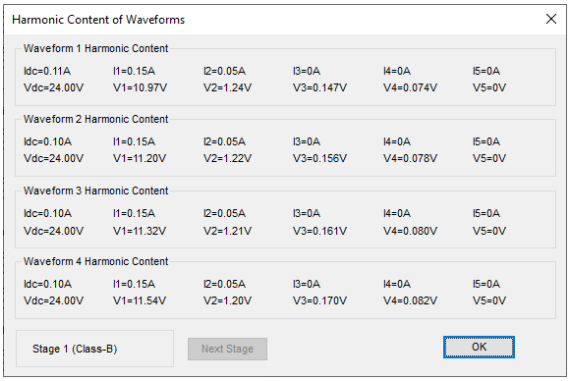


Figure 11. When the Waveform Components command in Figure 10 is selected, the waveform components are listed for the four sets of passband waveforms created when the ADW circuit is analyzed.

The Waveform Components command in Figure 10 will be active when the circuit has been analyzed with the actual harmonic terminations in place. When this command is selected, the components present in the four sets of passband waveforms created when the circuit is analyzed are listed (see Figure 11). The harmonic content listed can be compared with that obtained in a harmonic-balance simulation. Adjustments can then be made to the ADW harmonic content weight factors to improve the correlation.

The HC Search Results command in Figure 10 will be active when a systematic search has been performed for the optimum harmonic content of the transistor in a single-stage amplifier circuit. Optimum content implies the content that will ensure the best correlation with the results obtained in the harmonic-balance simulation.

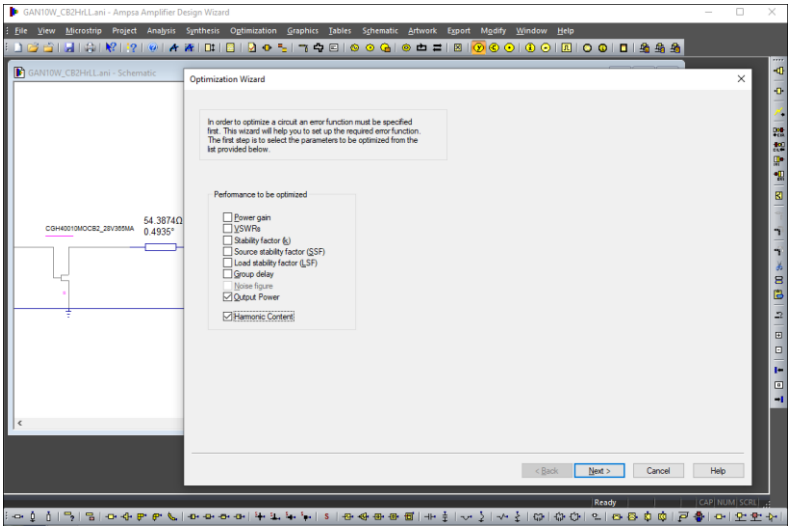


Figure 12. The option to optimize the harmonic content of the transistor used in a single-stage amplifier was selected here. The Optimization Error Function toolbar command was used to launch the Optimization Wizard.

If the Power and Harmonic Content options were selected on the first page of the Analysis Module Optimization wizard (see Figure 12), the option to perform a harmonic content search is provided on the Power page of the Optimization wizard (see Figure 13). The ADW harmonic content weight factors can be constant over frequency or can change linearly over the passband. Bounds can be set on the weight factors by using the Set Boundaries command.

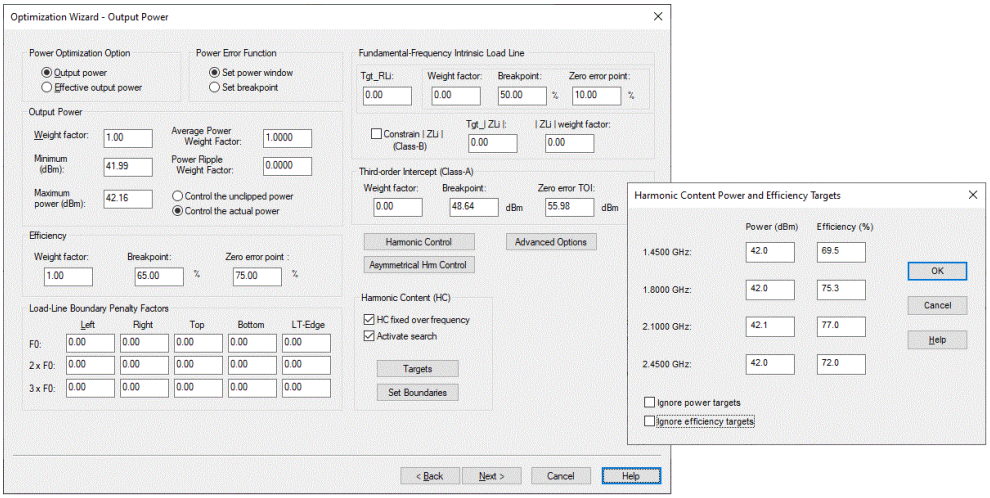


Figure 13. The harmonic content options provided on the Power page of the ADW Optimization wizard.

In addition to targeting a window of power levels, and efficiencies above a specified minimum, the measured power and efficiency at four passband frequencies can also be targeted when the harmonic content is optimized. (In the absence of measured data, harmonic-balance results can be used.) The four frequencies are automatically set by the ADW and are also the frequencies at which graphs for the intrinsic dynamic load lines can be displayed (lowest and highest passband frequencies, and two frequencies inside the passband). Note that the power or efficiency targets can be de-activated by using the options provided (see Figure 13).

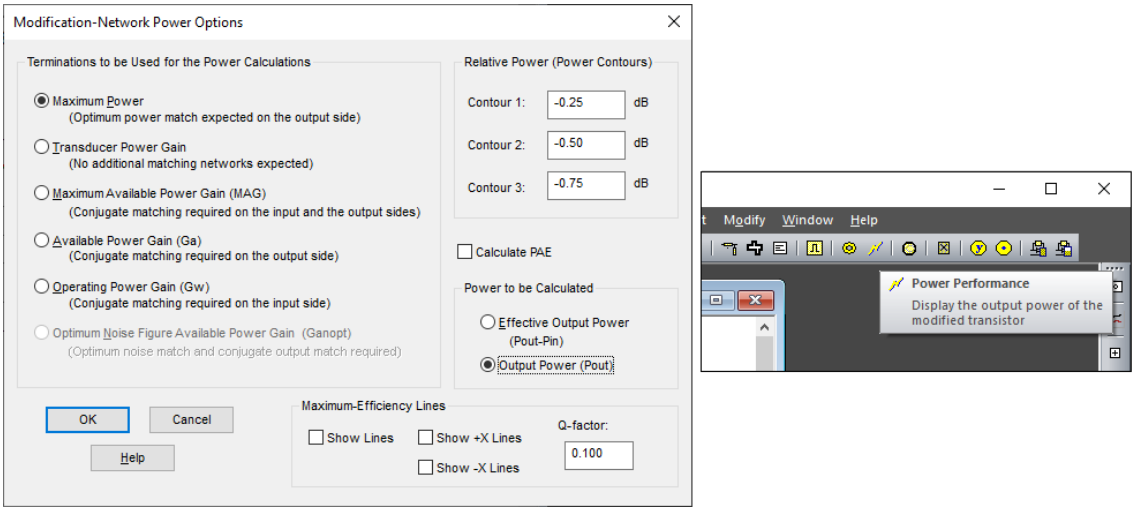


Figure 14. The power options provided for a modification network in the *S*-parameter module.

When a model has been fitted in the *S*-parameter module, the power and efficiency can be calculated by first setting the passband of interest (Modify Passband toolbar command) and then using the Power Performance toolbar command (see Figure 14). The contours targeted when the Power Options were specified are displayed graphically (see Figure 15). The contours

at the lowest passband frequency are shown in green, while magenta is used for the highest passband frequency. Note the anti-clockwise rotation of the contours.

DMS - STAGE ZL, Po and GAIN (PoM):

FREQUENCY (GHz)	LOAD TERMINATION (Ohm)		OUTPUT POWER (dBm)	POWER GAIN (dB)	Efficiency (%)
2.00000	11.55	+j0.03	43.493	20.570	44.34
2.10000	11.48	-j0.14	43.491	20.131	44.33
2.20000	11.30	-j0.25	43.490	19.735	44.32
2.30000	11.11	-j0.38	43.489	19.357	44.30
2.40000	10.93	-j0.51	43.487	18.995	44.29
2.50000	10.74	-j0.65	43.486	18.649	44.28
2.60000	10.56	-j0.81	43.484	18.316	44.26
2.70000	10.38	-j0.98	43.483	17.996	44.24
2.80000	10.20	-j1.16	43.481	17.688	44.23
2.90000	10.03	-j1.34	43.479	17.392	44.21
3.00000	9.86	-j1.54	43.477	17.105	44.19
3.10000	9.69	-j1.74	43.475	16.829	44.17
3.20000	9.53	-j1.96	43.474	16.562	44.15
3.30000	9.37	-j2.18	43.471	16.303	44.13
3.40000	9.22	-j2.41	43.469	16.052	44.11
3.50000	9.06	-j2.65	43.467	15.810	44.08
3.60000	8.93	-j2.90	43.465	15.574	44.06
3.70000	8.79	-j3.15	43.462	15.345	44.04
3.80000	8.65	-j3.41	43.460	15.123	44.01
3.90000	8.53	-j3.68	43.457	14.907	43.99
4.00000	8.40	-j3.95	43.455	14.697	43.96

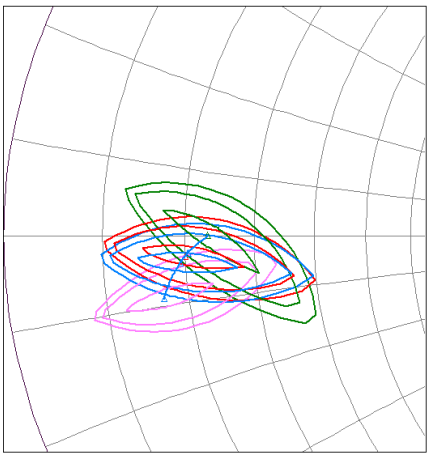


Figure 15. The performance with the peak power load termination is listed in table shown. Constant output power contours for a 2 – 4 GHz passband are displayed in the graph.

The main steps in fitting an ADW transistor model are summarized below.

Procedure for Fitting a Model to a Transistor in the ADW

1. Start the ADW and open a new ".spi" file (see Figure 4). Include the transistor name, the intended class of operation and the *dc* operating point in the file name (Example: "CGH40025CA_28V1800mA.spi").
2. Import a set of class-A *S*-parameters for the transistor into the document. Interpolate the *S*-parameter data to have data at the lowest and highest passband frequencies (Data | *S*-parameters menu command).
3. Define the artwork vectors by using the Data | Artwork Vectors menu command. The artwork vectors define the positions and orientations of the connections to be made to the transistor.
4. Use the Data | Transistor Model menu command to fit a class-A model to the imported *S*-parameters. Start by first initializing the intrinsic components (limit the frequency range to lower frequencies), and then specify small values for the expected extrinsic components. Use the Optimize command to optimize the model components over the frequency range covered by the imported *S*-parameters. Constrain the element values during the optimization. First fit the *Y*-parameters with the least-square error function and proceed to the *S*-parameters and the L_1 error function when a reasonable fit has been obtained.
5. Calculate the parameters for the lines defining the *I*/*V*-plane boundary area for the intrinsic load-line. *I*/*V*-curve information can be used to decide the boundary area. If no curves are available, estimates can be used. These estimates can be fine-tuned to get the power and efficiency expected.
6. Specify the *dc* operating point, select the class of operation (class-A in this case), and specify the other parameters of interest. The compression factors can initially be set to 3 dB for class-A, Class-B, and class-F operation, and to 0.5 dB for inverse class-F and class-B2 operation. Zero values can initially be used for the efficiency fitting factors.
7. Calculate the expected maximum power and the associated efficiency by first setting the passband of interest (Modify Passband toolbar command) and then using the Power Performance toolbar command (see Figure 14). Compare the performance with that

stated in the data sheet or obtained in a harmonic-balance simulation. Adjust the model to improve the correlation, if necessary.

8. If the intended class of operation is not class-A, use the File | Save As Class-B menu command to convert the model for class-B operation. Modify the class and the other *I*/*V*-Boundaries page specifications for the intended class of operation. Calculate the expected maximum power and the expected efficiency as done before in Step 7, compare the results with those expected and make modifications as required.
9. Change the current in the file name to the peak current targeted instead of the *dc* operating current (File | Save As menu command).
10. Use the Export | ADW Circuit File | Save menu command to create an ADW circuit file (".ani") for the transistor. Open this circuit file (The file can be found in the Project Directory defined with the Analysis Module File | Settings menu command.), double-click the transistor label and switch to using the transistor model instead of the set of *S*-parameters stored in the circuit file. Refer to Figures 16 and 17 for the details.

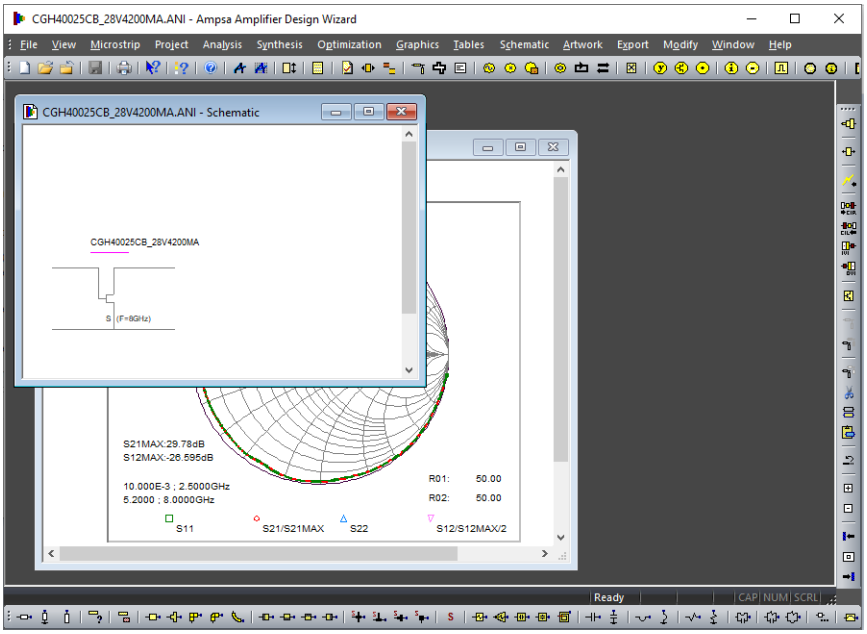


Figure 16. The circuit file exported in the *S*-parameter module has been opened in the Analysis module.

11. Use the Project | Transistor Models Used menu command to open the Transistor Modeling wizard, select the *I*/*V*-Plane Boundaries tab and then select Other Harmonics. Set the other harmonics appropriately. The (initial) specifications set for a class-B stage are shown in Figure 18.
12. To proceed with designing a load matching network for the transistor, first set a passband by using the Project | Frequencies menu command. If harmonic control will be used, be sure to include the harmonics of interest in the frequency list. If not set already, the File | Settings command can be used to set the Data, Project, and Export Directories for the project. Use the Project | Options menu command to set the default dimension units for the project. A substrate can be defined by using the Project | Substrates menu command. If the circuit terminations will not be 50Ω, use the Project | Terminations menu command to define the terminations. Pads for mounting the transistor can be added by using the transmission line commands provided on the Schematic toolbar. The dimensions of the pads can be edited by switching from the schematic view to an artwork view (Artwork View toolbar command).

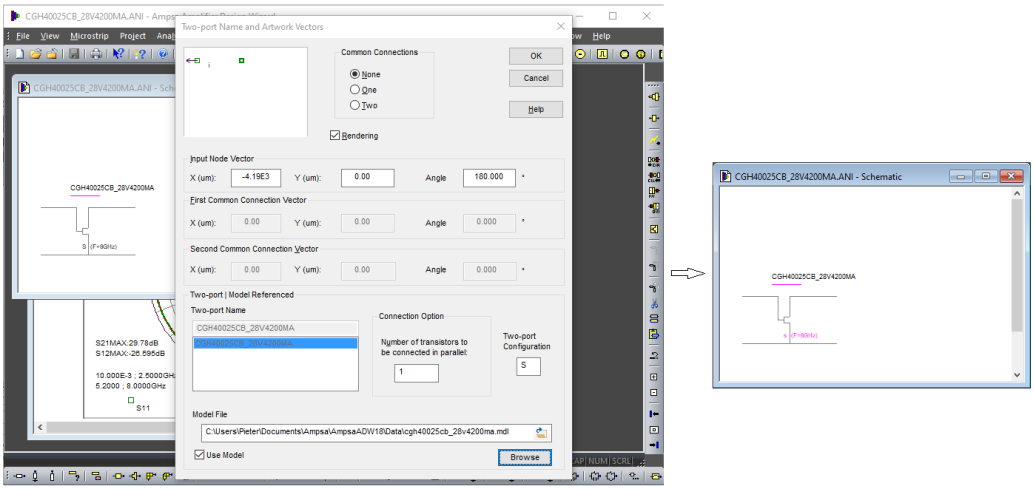


Figure 17. The transistor label in the schematic was double-clicked to change from using the set of *S*-parameters in the circuit file to using the transistor model instead. Note that the transistor configuration (S for common source) is now displayed in magenta.

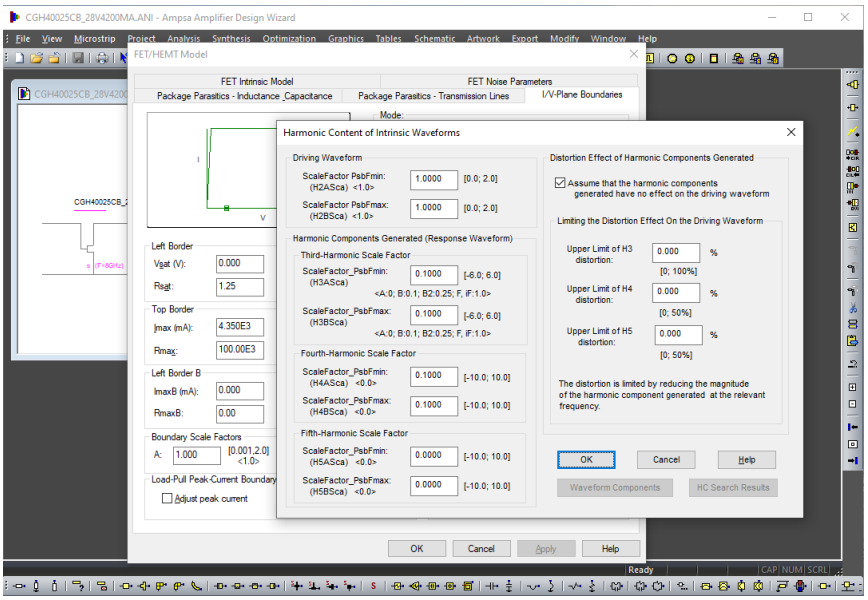


Figure 18. The harmonic weight factors for a class-B transistor model were set here. Low third harmonic and fourth harmonic and zero fifth harmonic content were assumed. The second harmonic content of the output driving waveform was not modified and the harmonics generated in the response waveform are assumed to have no effect on the driving waveform (no distortion).

13. The design can be started by first designing the load matching network, but a better approach may be to stabilize the transistor first. The transistor can be stabilized by adding lossy sections on its input side. These sections can be combined with series transmission lines to obtain the desired degree of stability, to level the gain and to improve the input VSWR. Note that one or more series transmission lines with low characteristic impedances are usually required between the transistor and any series connected lossy section. The purpose of these lines is to improve the poor input VSWR of the transistor before adding the series lossy section. (Move the transistor reflection coefficients from the edge of the Smith chart towards the centre of the chart.) The most efficient design path is usually to experiment with the series transmission line required first and then to set up a suitable stabilization network and optimize it (see Figure 19). If the load network has not been designed yet, it is necessary to decide on the gain to

be used in the optimization (MAG or operating power gain). Select the gain that yields the most power. Note the Stability Factors, Shunt Stabilizing Resistance, Series Stabilizing Resistance and VPF Stabilizing Resistance commands provided in the Tables menu of the Analysis Module. These commands can be used to decide on appropriate initial values for the stabilization components.

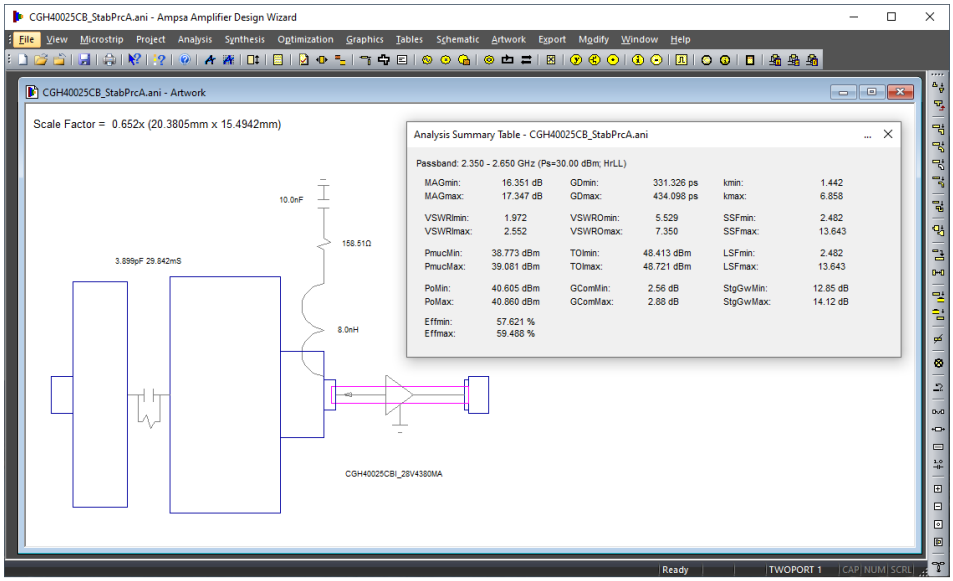


Figure 19. The stabilization network shown was designed by using the ADW Optimization wizard.

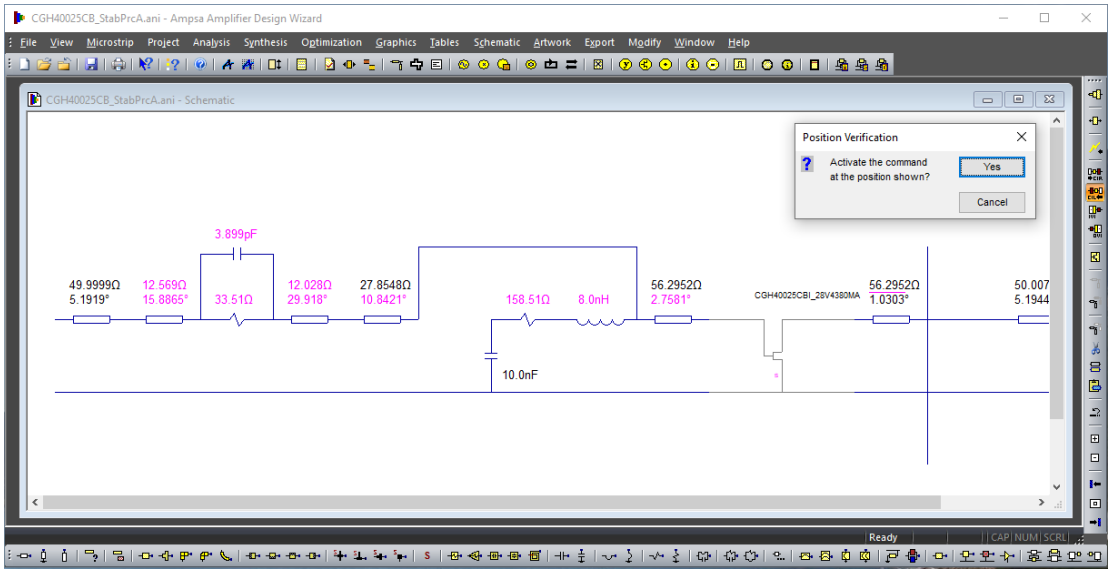


Figure 20. The CIL command was selected on the Synthesis toolbar to set up the specifications for the load network of the single-stage amplifier to be designed.

14. Use the CIL command on the Synthesis toolbar to set up the specifications for the load matching network (see Figure 20). The matching network required can be synthesized by using the Impedance-Matching wizard or one of the CMA wizards. (Wizards for designing phase-controlled matching networks. Synthesis is for a specific passband frequency and a conjugate match is assumed at that frequency [6].)
15. Use the Insert Matching Network wizard on the Synthesis toolbar to design the input matching network. When this wizard is used, the network specifications are usually set

for gain levelling. When a power stage is designed, a good input VSWR may be preferred instead. When this is the case, set the transducer power gain to 1.0 by using the Specifications | Terminations menu command in the Impedance-Matching wizard. (To do this automatically, select the Slope Gain command and then set the highest passband gain and the gain slope to 0 dB.)

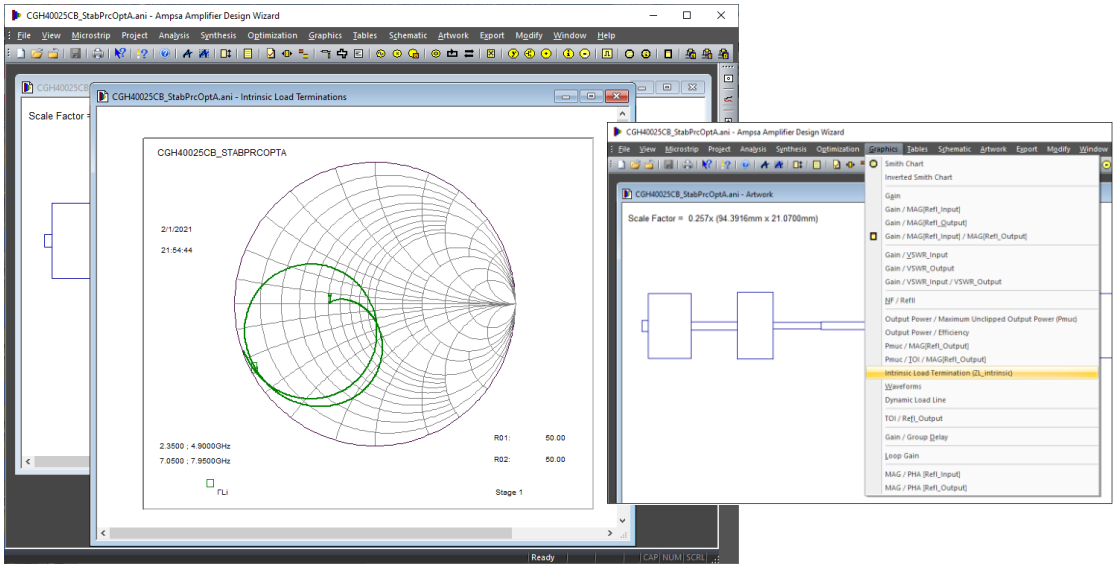


Figure 21. The intrinsic load impedance presented to the transistor by the load matching network of the single-stage amplifier. The menu command used to invoke the graph is shown on the right.

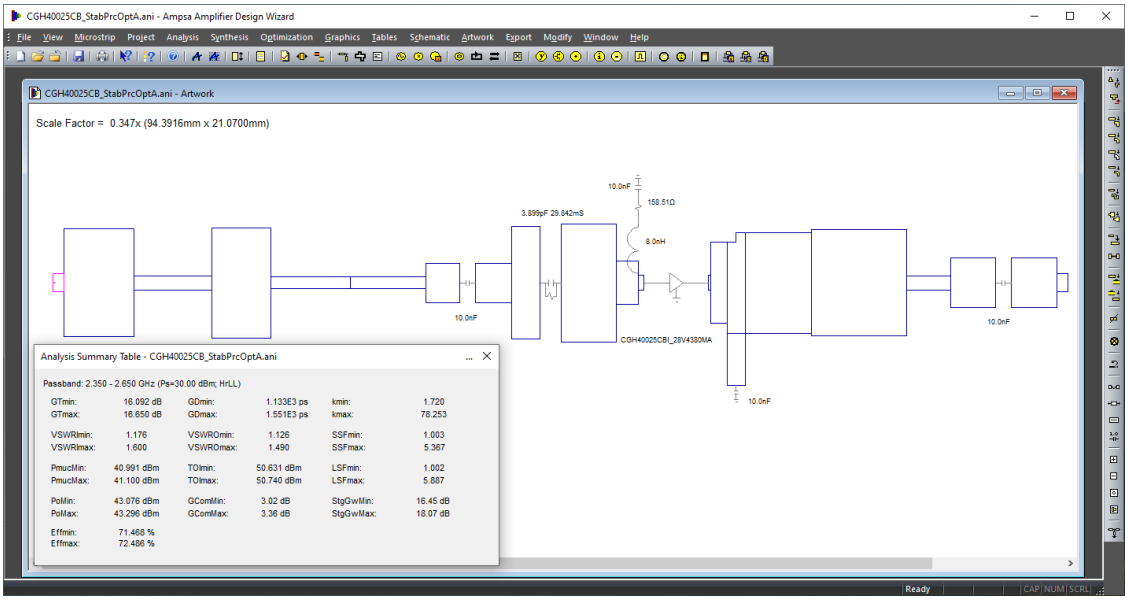


Figure 22. A single-stage class-B amplifier designed as described above. Commensurate impedance matching networks were synthesized for the amplifier by using the Impedance-Matching wizard. Except for some discrepancies in s_{11} and minor discrepancies in the efficiency, the correlation with a harmonic-balance simulation is excellent. (The electrical circuit was exported for simulation.) The length of the RHS pad for RC combination can be decreased to obtain a good input match in the harmonic-balance simulator (27.5° instead of 29.9°).

16. Switch to the HFLL analysis mode, verify that all the harmonic frequencies of interest are included in the frequency list (Project | Frequencies menu command) and analyse the circuit. If the performance is not as expected, check the intrinsic load line by using the Graphics | Intrinsic Load Terminations menu command and/or the Tables | Intrinsic

Load Terminations menu command (see Figure 21). If the harmonic terminations were ignored during synthesis, it is highly likely that the harmonic terminations will be off, and optimization will be required. Optimize the single-stage amplifier by using the ADW Optimization wizard.

17. Export the electrical description of the amplifier for simulation in a harmonic-balance simulator and adjust the transistor model to improve the correlation in the results, if necessary. When the compression is deep, adjustments may be required to the circuit exported to compensate for the change in s_{11} with compression.
18. Use the Export | Convert Circuit to Microstrip Form menu command in the ADW Analysis Module to convert the implicit microstrip junctions to explicit junctions. Open the exported ADW circuit file, analyse the circuit, and re-optimize the performance, if necessary. Export the ADW microstrip circuit and the ADW electrical circuit to the harmonic-balance simulator. (The circuit viewed is the circuit exported.) The microstrip models (X-models in Microwave Office™) in the harmonic-balance simulator may be more accurate than the models used in the ADW. Check the *S*-parameters of each microstrip matching or modification network (as calculated in the harmonic-balance simulator) against its electrical performance. Adjust or tune each network for a good fit to the *S*-parameters of the associated electrical network. If the correlation is not close for a network, follow the instructions in Step 19 for that network or the complete circuit.

    If some of the design rules in the harmonic-balance simulator are violated, corrections can be made to the ADW design. The widths of some of the lines in the ADW network may be too wide or too narrow, or higher order modes could be an issue. Some of the design rules may be overly cautious, and simulation in an EM simulator may be required to get a better idea of potential issues.

    Higher order modes can be suppressed by extending the ground plane towards the circuit, by using cavities and/or by using absorber material. Other options are to use a thinner substrate and/or to use a substrate with a higher relative dielectric constant. Higher order modes should be suppressed up to at least the third harmonic when a high-efficiency amplifier is designed.

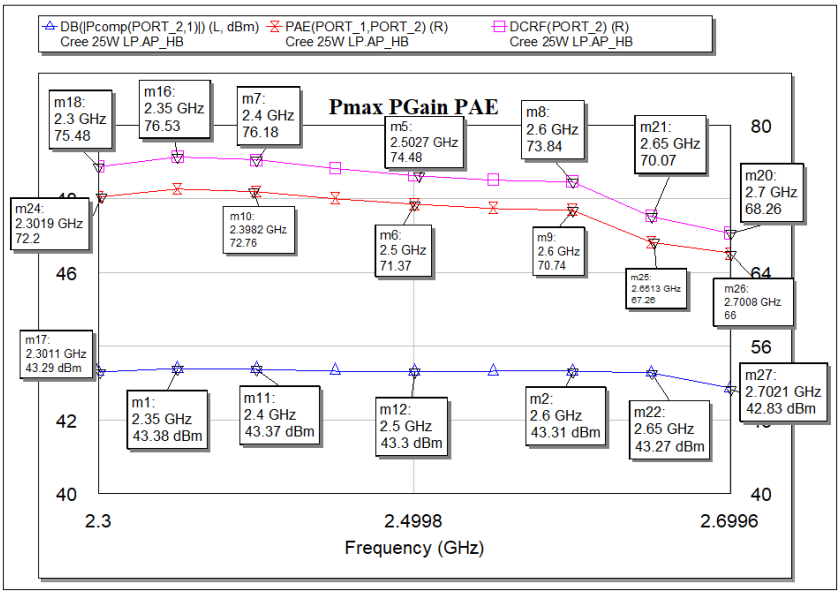


Figure 23. The Microwave Office™ power and efficiency for the ADW circuit in Figure 22.

19. Simulate the step junctions, any curves or bends, and the T-junctions and crosses used in the ADW circuit in an EM simulator (Sonnet Software's EM is recommended; the ADW can export Sonnet ".son" files), import the associated *S*-parameters into the ADW (Use the Junction *S*-parameter command provided on the Schematic toolbar) and replace the relevant junctions with *S*-parameter based models. The Export | Convert Circuit to Microstrip Form menu command can be used to convert the implicit microstrip junctions in the original ADW circuit to explicit *S*-parameter based junctions. When this option was used, a list of the discontinuities to be EM simulated is written to a text file when the ADW circuit with the *S*-parameter based discontinuities is analyzed. (The root part of the file name used is the circuit name extended by "_EMSreq.txt".) Re-optimize the ADW circuit and export the microstrip circuit to the harmonic-balance simulator for further processing.

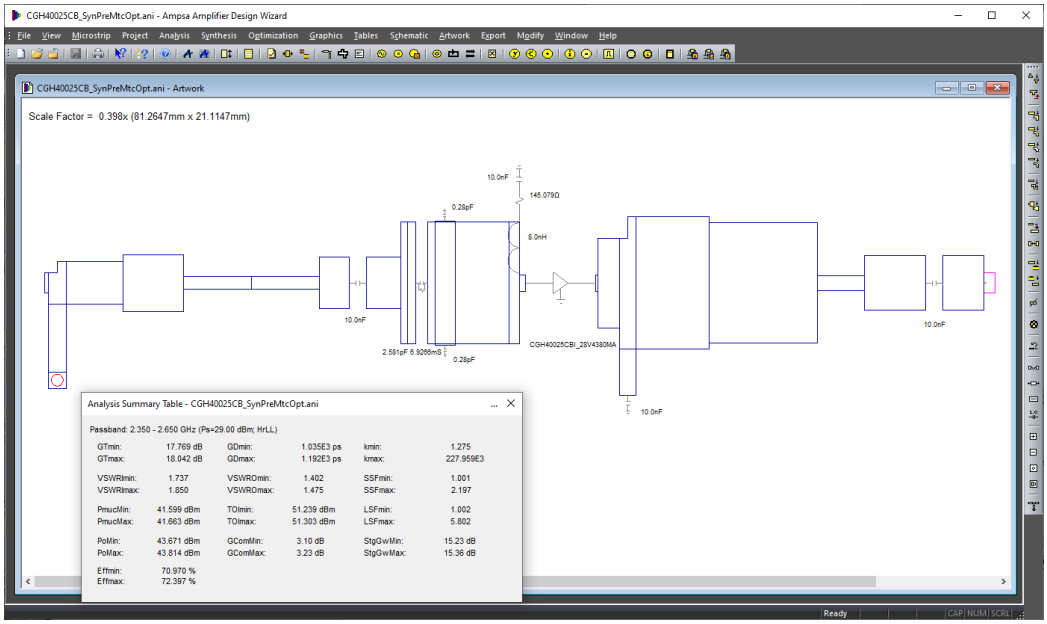


Figure 24. A single stage amplifier designed by synthesizing a CMA matching network for the input before adding the stabilizing sections.

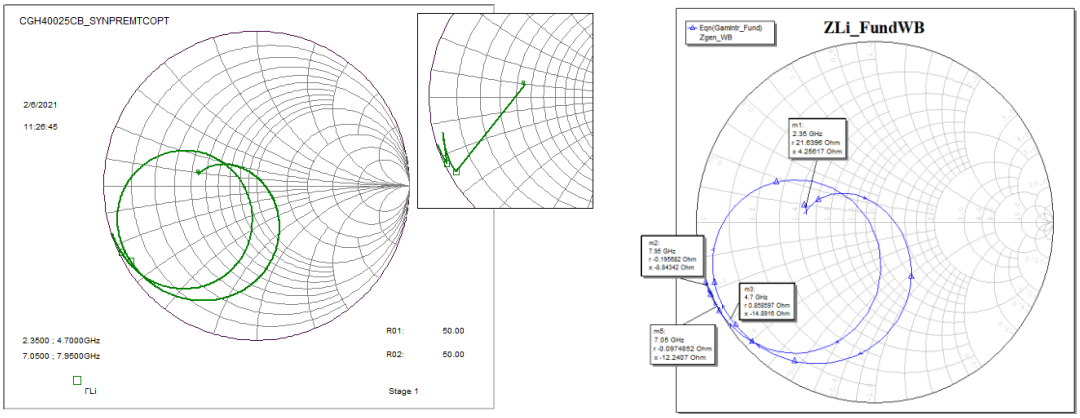


Figure 25. The intrinsic load line for the amplifier in Figure 24 as simulated in the ADW and in Microwave Office™.

The single-stage amplifier in Figure 22 was designed by following the approach outlined above. Another option for designing the stabilization network is to first explore using one of the CMA networks (phase-controlled matching networks) to lower the input VSWRs and then to add the series lossy section. The amplifier shown in Figure 24 was designed by following this approach. (The gain of this amplifier is higher than that of the amplifier shown in Figure

22.) The intrinsic load line in the ADW is compared with that obtained in Microwave Office™ in Figure 25. (The correlation is usually tight.) The performance of the ADW circuit obtained in Microwave Office™ is shown in Figure 26.

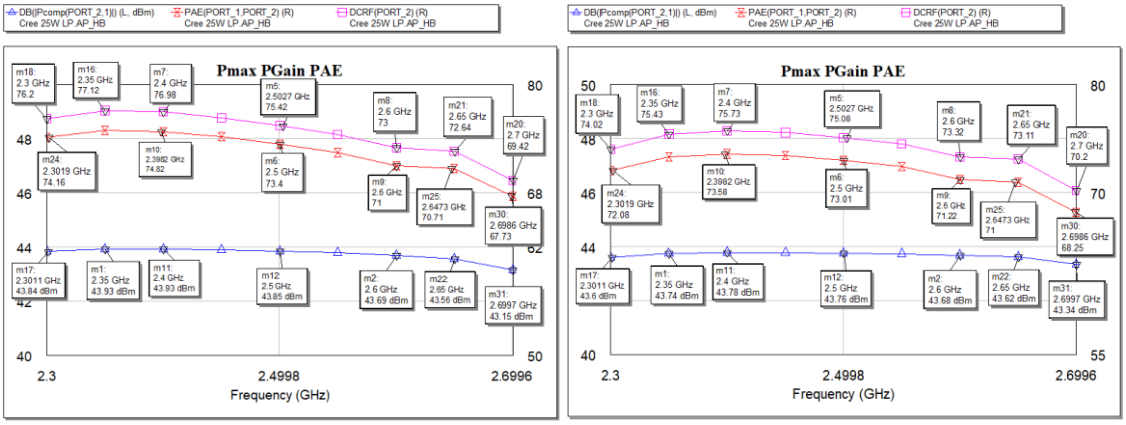


Figure 26. The performance of the amplifier in Figure 24 as simulated in Microwave Office™ with the non-linear model for the transistor. The performance shown on the right was obtained by tuning the line to the right of the RC section in the input matching network (tuned to improve the large-signal s_{11}).

Note that the gain compression shown for both amplifiers correlates well with that obtained in Microwave Office™.

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