Ampsa ADW Version 23 Features

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The Amplifier Design Wizard (ADW) is a synthesis tool for RF and microwave impedance-matching networks and amplifiers. The focus in the ADW is on controlling the intrinsic load terminations presented to the transistors used. In doing so the modes of operation are also controlled. When available, load-pull or source-pull targets can also be used in the ADW.

A structured design approach is provided in the ADW. Amplifiers are designed stage by stage by using lossless impedance-matching networks, as well as lossy sections (resistive loading and/or feedback sections). Lossy sections are required for stability and gain levelling, as well as for reducing the gain-bandwidth constraints of wideband impedance-matching problems. Small-signal amplifiers (low noise or low power), as well as high-efficiency amplifiers can be designed with the ADW.

For high accuracy, external EM simulation of at least the microstrip discontinuities in an ADW circuit is required. The EM *S*-parameters can be used directly in ADW *S*-parameter based junction models or can be used to optimize the parameters of the standard discontinuity models used in the ADW. To make the process efficient, the implicit discontinuities in an ADW circuit can be separated out automatically and can then be exported for EM simulation. The ADW artwork can be exported to Sonnet Software®'s EM, or via ".bas" script to Microwave Office™ and via DXF to other CAD packages. If the naming conventions used are maintained, the simulation results can be imported back into the ADW with minimal effort.

ADW circuits are usually exported to a harmonic-balance simulator for further processing. Measurements or the results obtained with harmonic-balance non-linear transistor models can be used to fine-tune the transistor models fitted in the ADW.

A set of wideband *S*-parameters and the information generally available in data sheets are required to fit a transistor model in the ADW. *DC* or pulsed *I*/*V*-curves are required to set accurate boundaries for the allowable intrinsic load line area, but if these curves are not available, estimates can be used. The power and efficiency calculations and the load-pull capabilities (CIL wizard; see Figure 1) in the ADW are based on clipping theory [1]. With five boundary lines defining the allowable load line area and the introduction of power parameters to map the intrinsic load termination to the external terminations [2], clipping theory has been extended to a fully useful point in the ADW. A compression curve [3] and fitting factors are used to model the compressed behaviour.

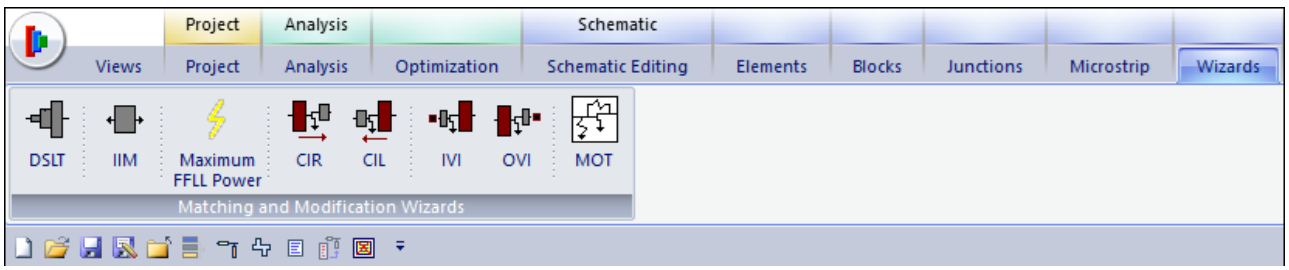

Figure 1. The impedance-matching and modification networks wizards provided in the ADW.

Coefficients for a typical $C(V)$ profile can be specified in the ADW for the output capacitance (C_{ds}) of a transistor. The effect of this nonlinearity on a design [4, 5] can then be evaluated in the ADW and the design can be optimized for this effect, if necessary.

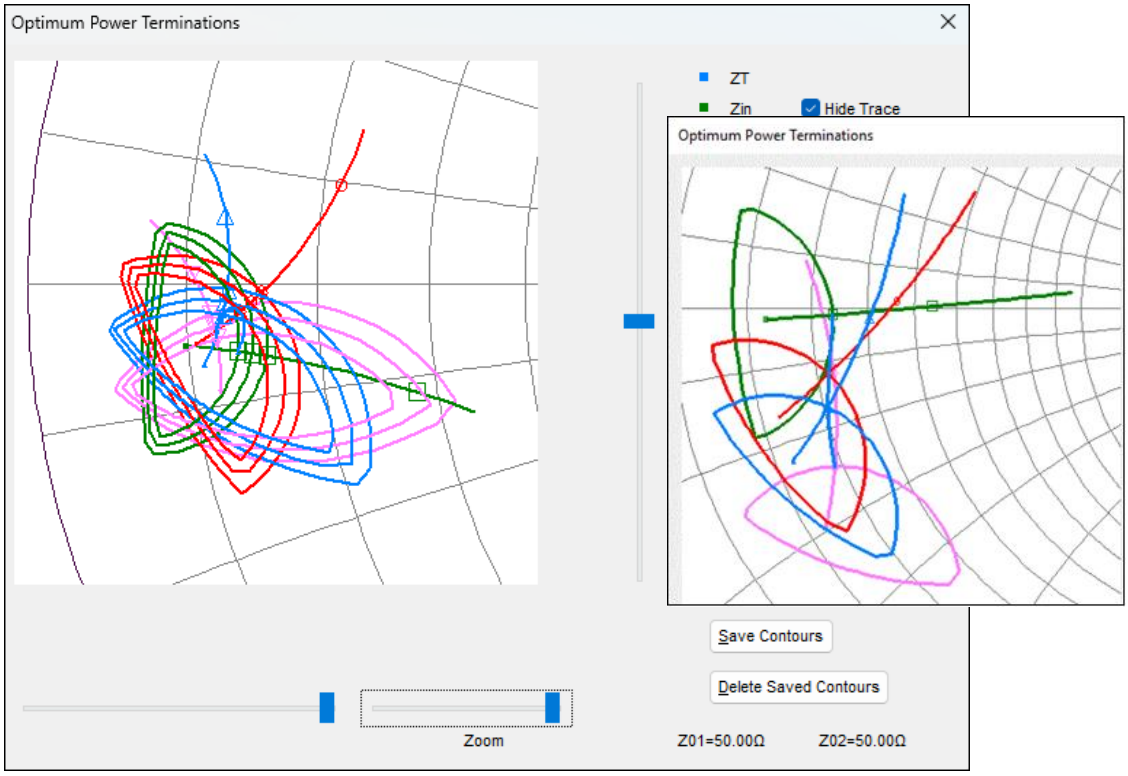

Figure 2. Examples of the ADW constant power contours and maximum efficiency lines.

Extensive impedance-matching capabilities [2] are provided in the ADW. The fundamental-frequency performance, as well as the second-harmonic performance and the third-harmonic performance can be controlled. The targets at the fundamental frequencies can be points or circles, while a reactance range or a Smith chart sector can be targeted at each harmonic. The CIL wizard can be used to setup the specifications for the load impedance-matching network of a power transistor. It can also be used to setup interstage-matching problems. The IIM wizard (see Figure 1) is used to setup the specifications for the input matching network.

The ADW can define target areas for the load matching network of a transistor by using continuous-mode theory [6, 7, 8], or by using power contours and maximum-efficiency lines or areas [9]. The reference plane for all the targets is the insertion point of the matching network. Power parameters [2] are used to map the intrinsic terminations to the associated terminations at the insertion point.

Instead of targeting the external harmonic terminations, the intrinsic harmonic terminations can also be targeted directly in Version 23 of the ADW. The harmonic targets of interest are the intrinsic terminations, and eliminating the distortions introduced by the mapping in the error functions yields better results when matching networks are synthesized or optimised.

Constant output power or constant effective output power contours can be created by the CIL wizard. The best efficiency point on each power contour is marked by the maximum efficiency line (see Figure 2). The maximum efficiency line is on the voltage clipping side of each power contour. The intrinsic load impedance is purely resistive on the maximum efficiency line. Two additional lines can also be created for the minimum acceptable efficiency. The intrinsic load reactance is positive on one of these lines and negative on the other (see Figure 3).

The minimum acceptable (drain) efficiency targeted in the Figure 3 example was 58%. The power in the highlighted section is higher than the power specified for the lowest power contour and the efficiency is higher than 58%.

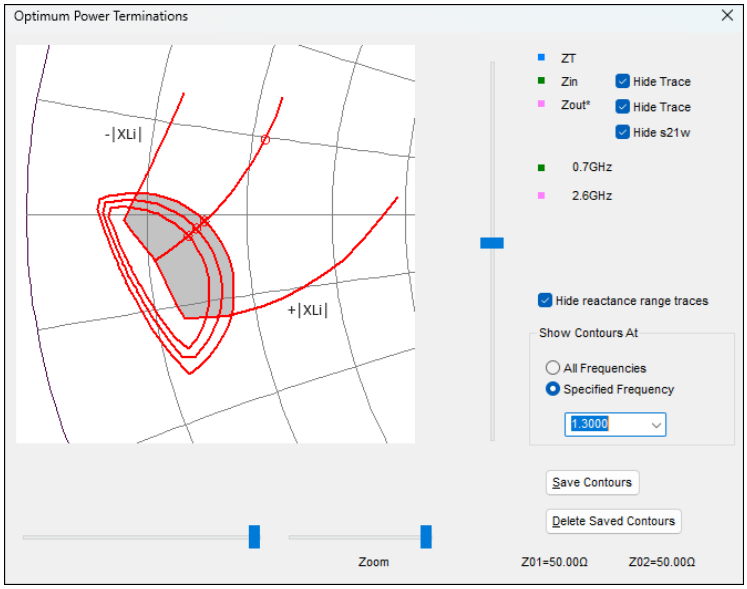

Figure 3. ADW constant power contours and the efficiency lines for a transistor at 1.3GHz. The power in the highlighted section is higher than the power specified for the lowest power contour and the efficiency is higher than the minimum acceptable efficiency specified.

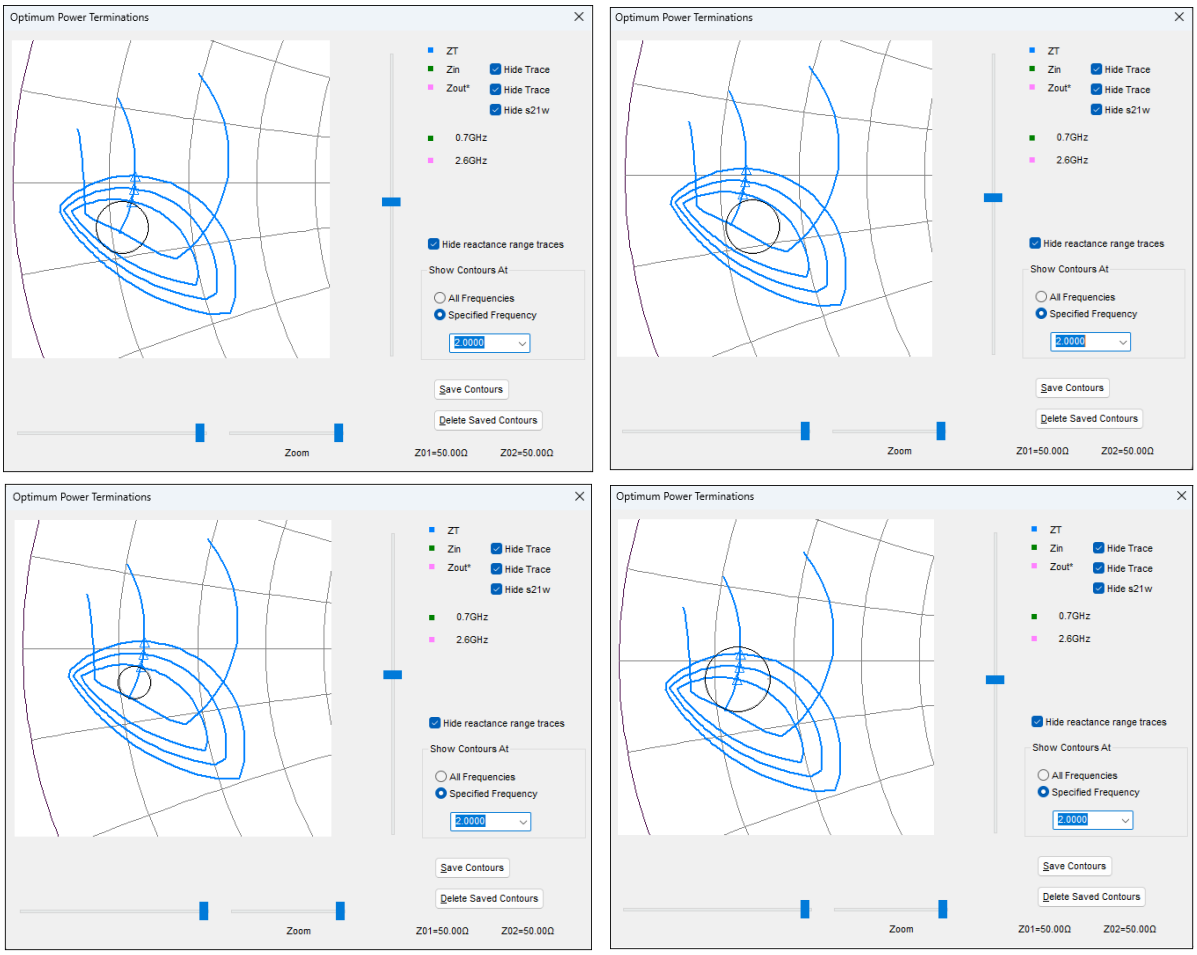

Figure 4. The different options provided for fitting a circle to be used as a fundamental-frequency target in the matching module of the ADW.

The ADW can fit circles to the areas defined by the contours targeted and the efficiency lines used. The circles fitted are classified in four categories (See Figure 4). Type A and type B circles are fitted to the contours targeted. A type A circle is centred on the peak power point, while a type B contour is centred on the contour itself. The diameter of a type C circle is defined by the optimum efficiency point on the contour targeted and the peak power point. The centre of a type D circle is the optimum point (usually the point with highest efficiency) on the contour targeted. The minimum acceptable efficiency lines and the maximum efficiency line are used to define the radius of a type D circle. When a type D circle is fitted, the intrinsic load reactance can be constrained to be only inductive or only capacitive (see Figure 5). Type D circles restricted to inductive intrinsic load terminations were fitted to the contours and efficiency lines shown in Figure 6.

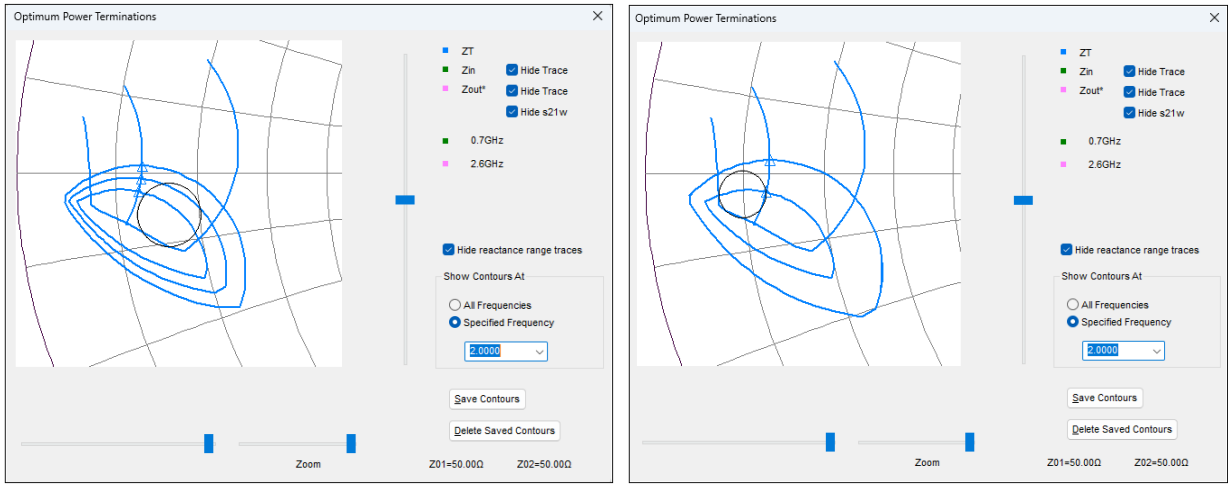

Figure 5. Type D circles restricted to inductance (LHS) and capacitive (RHS) intrinsic load impedances.

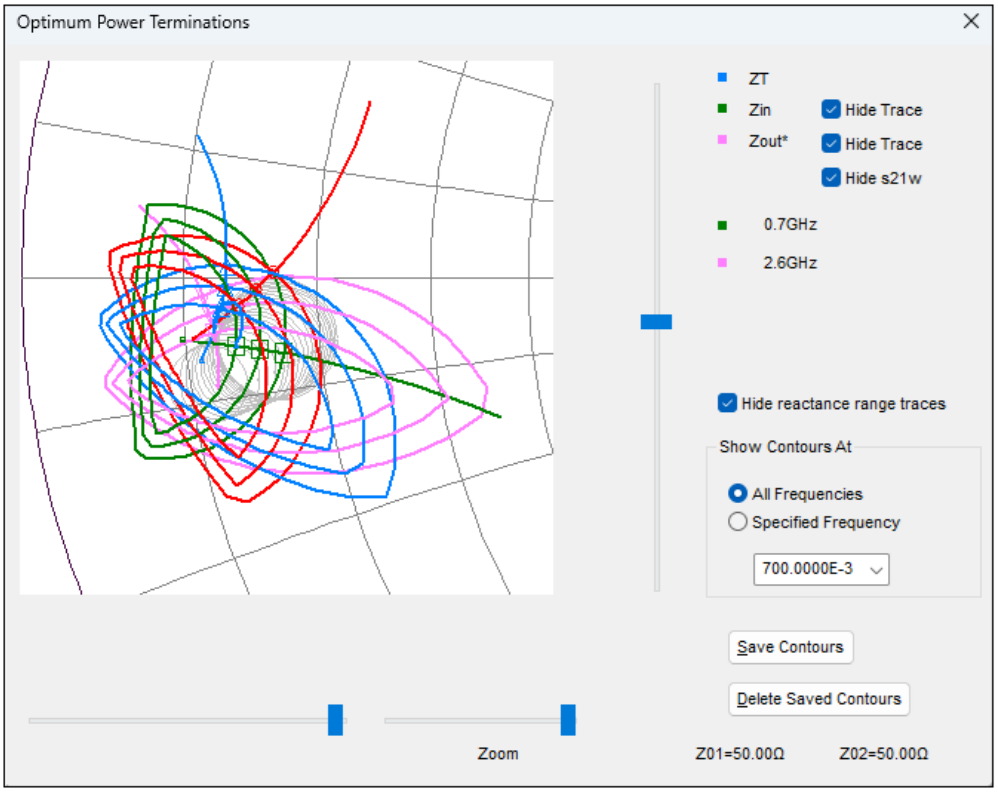

Figure 6. Type D circles restricted to inductive intrinsic load terminations were fitted to the power contours shown here.

In addition to the power contours and efficiency lines, various options are also provided in the ADW to control the intrinsic load terminations directly. These include setting targets for standard Class-B, Class-B/J, Class-F, and inverse Class-F operation, as well as the associated continuous classes. The second-harmonic clipping contours technique [8] has also been implemented in the ADW. Targets can also be set for Class-B2 operation. (Approximate half-sinusoids for both the intrinsic output voltage and the intrinsic output current.)

The approximate intrinsic opens or shorts required in some classes of operation can be a problem if the passband is relatively wide. If an exact intrinsic open or short is targeted over the passband, the reflection coefficient required at the external reference plane will rotate anticlockwise with increasing frequency. This is an issue because passive networks can only provide clockwise rotation. Clockwise rotation may be obtained if low or high impedances with clockwise rotation of the reflection coefficient are targeted instead (see Figure 7).

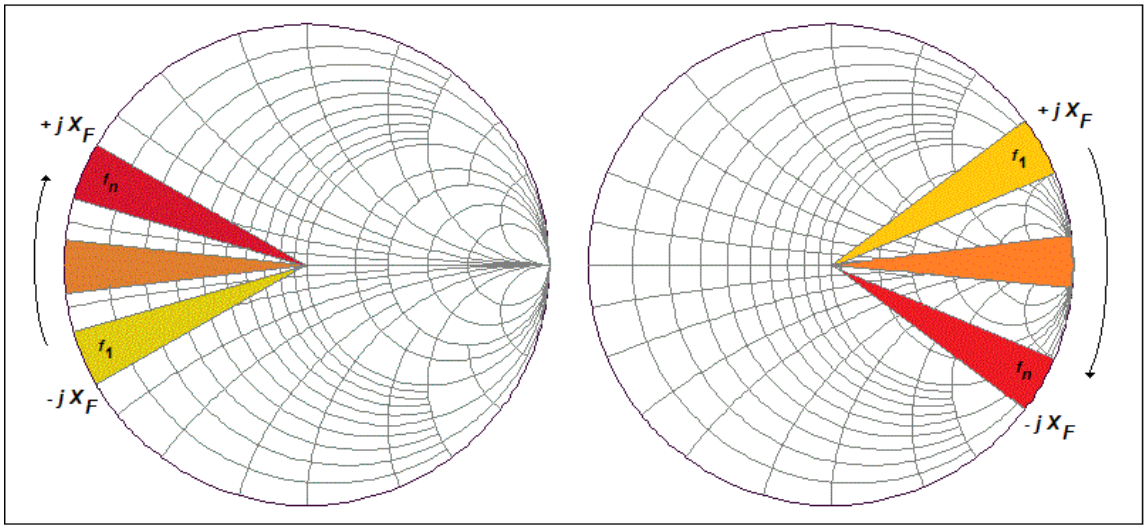

Figure 7. When approximate shorts or opens are required at all the frequencies in a harmonic band, the option to target clockwise rotation of the second harmonic and the third-harmonic targets with increasing frequency is provided.

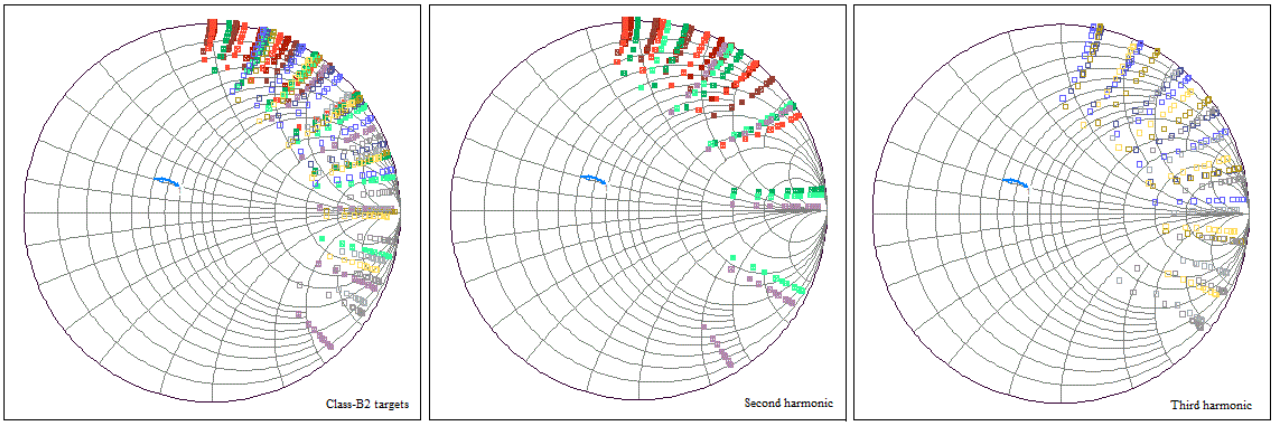

Figure 8. An example of the fundamental-frequency (blue trace) and second and third harmonic targets (harmonic markers) generated for a class-B2 amplifier stage.

Fundamental-frequency and second- and third-harmonic targets for the load matching network of a Class-B2 amplifier stage are shown in Figure 8. The rotation of the harmonic targets is clockwise with increasing frequency for both the second and third harmonics. Exact intrinsic shorts or opens are not required in a class-B2 stage at the second or the third harmonics.

Second-harmonic clipping contours [8] can also be plotted in the ADW. With the intrinsic output current of the transistor assumed to be an undistorted half-sinusoid of fixed amplitude and intrinsic shorts at the third and higher harmonics, a clipping contour defines the second-harmonic area for no distortion in the voltage waveform (that is, $V_o(t)$ >= 0.0) when a specific intrinsic fundamental-frequency load impedance is targeted. In the ADW, the clipping contours are clipped at the edge of the Smith Chart, but the actual contours will extend into the negative resistance area.

The clipping contours were derived for an ideal transistor. Any boundary line (knee) effects were ignored. To allow for the reduction in the voltage swing because of clipping on an intrinsic *I*/*V*-plane boundary line (see Figure 9), the effective *dc* voltage should be used in the clipping equations instead of the actual *dc* voltage. The effective *dc* voltage is the difference between the actual *dc* voltage and the boundary line intercept voltage for the load termination used (V_k, V_e or V_t in Figure 9). The clipping contour current level is also set by the intercept point (I_k, I_e or I_t).

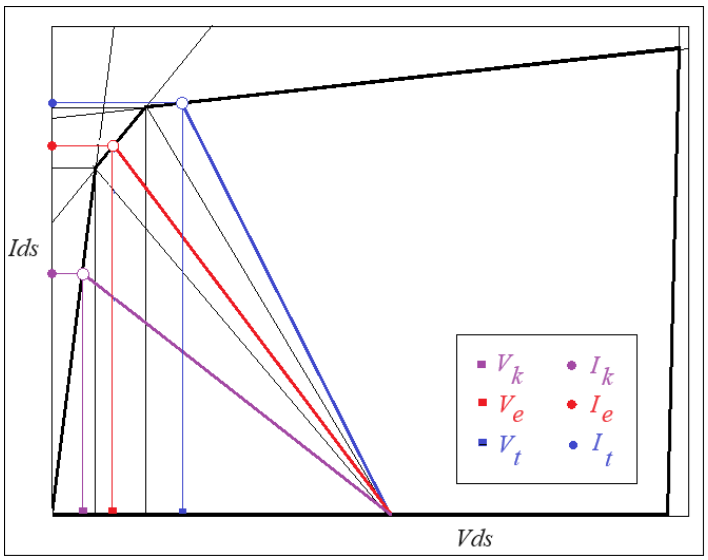

Figure 9. The effective *dc* voltage and the current to be used for a clipping contour are set by the boundary line intersect with the intrinsic load resistance.

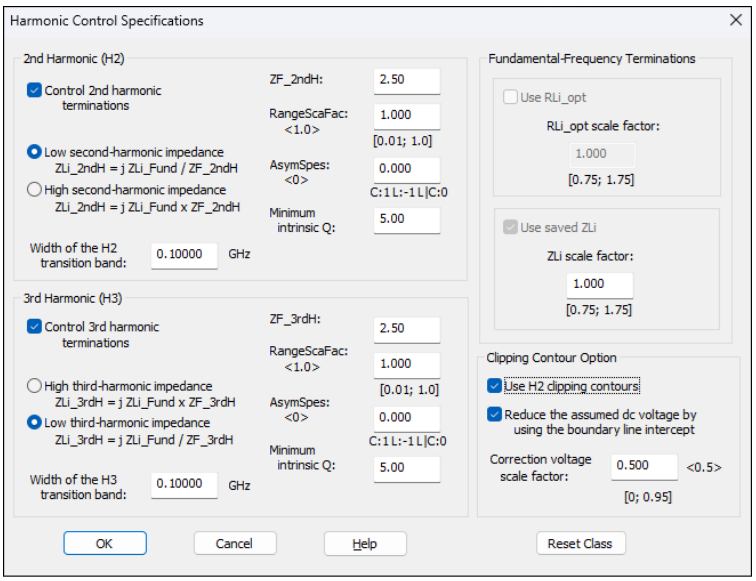

Figure 10. The harmonic control options provided in the ADW for the base classes. The clipping contour options are provided for Class-B and Class-F stages.

If the effective *dc* voltage is used in the clipping contour equations, the clipping contours will just touch the Smith chart edge and there will be no positive resistance second-harmonic clipping area. Allowance is made for a scale factor in the ADW to scale the correction applied to the clipping contour *dc* voltage down to a value lower than the boundary intercept voltage (see Figure 11). This will leave some excess voltage in place for the clipping contours. If hard clipping is assumed, there can be no excess voltage. Interaction with the knee will allow for some excess (wave shaping). To minimize distortion and loss in performance (power and efficiency), the excess should be kept as small as possible for the passband targeted. Because the excess voltage allowed has no real basis, the performance will be degraded for points away from the optimum and deeper into the clipping area. The usefulness of the clipping contours is in limiting the degradation in the performance while extending the target areas or angular spans for the harmonic control (no free pass).

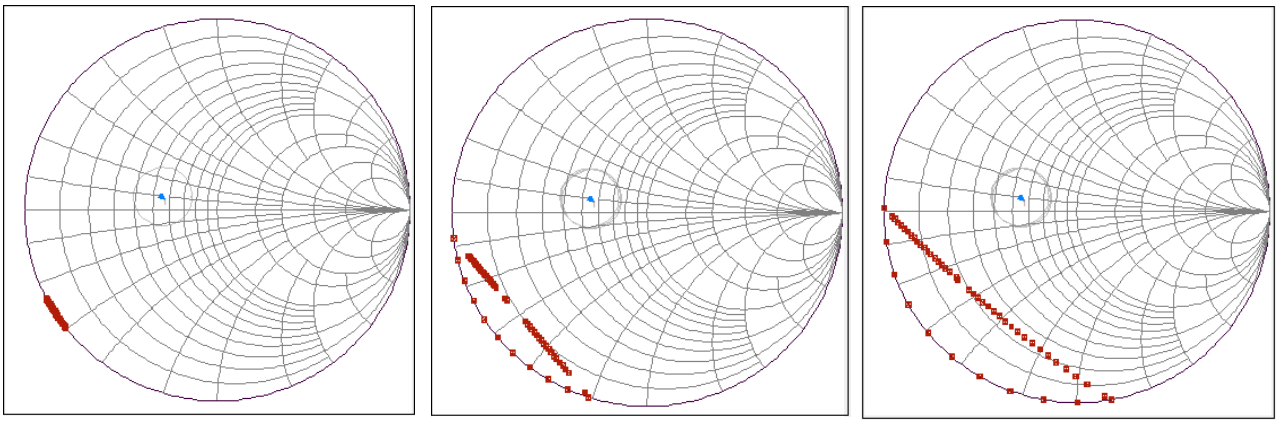

Figure 11. The positive resistance clipping contour area is proportional to the excess voltage specified in the clipping contour equations. If hard clipping on the boundary lines is assumed, there will be no excess voltage. The scale factors used for the correction voltages were 0.95, 0.5 and 0.0, respectively.

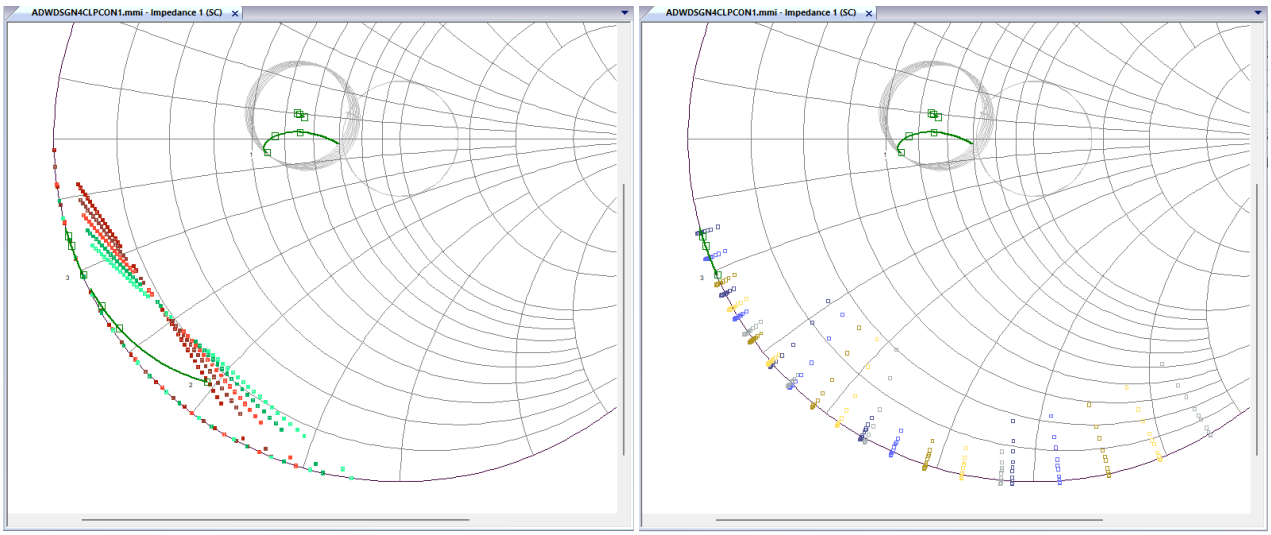

Figure 12. The input reflection coefficients of a matching network designed with second-harmonic clipping contours are shown here with the clipping contours on the left and the third-harmonic targets on the right.

A narrowband (1.0 – 1.4 GHz) second-harmonic clipping contour example is provided in Figure 12. The clipping contours at four frequencies in the passband targeted are shown (red to green harmonic markers). The blue to yellow harmonic markers are used for the third-harmonic intrinsic terminations targeted (approximate shorts). The green traces marked 1, 2 and 3 are the reflection coefficients of a matching network at the fundamental frequencies and the second and third harmonics, respectively. The intrinsic load impedances and the dynamic load lines for the clipping contour network synthesized are shown in Figure 13.

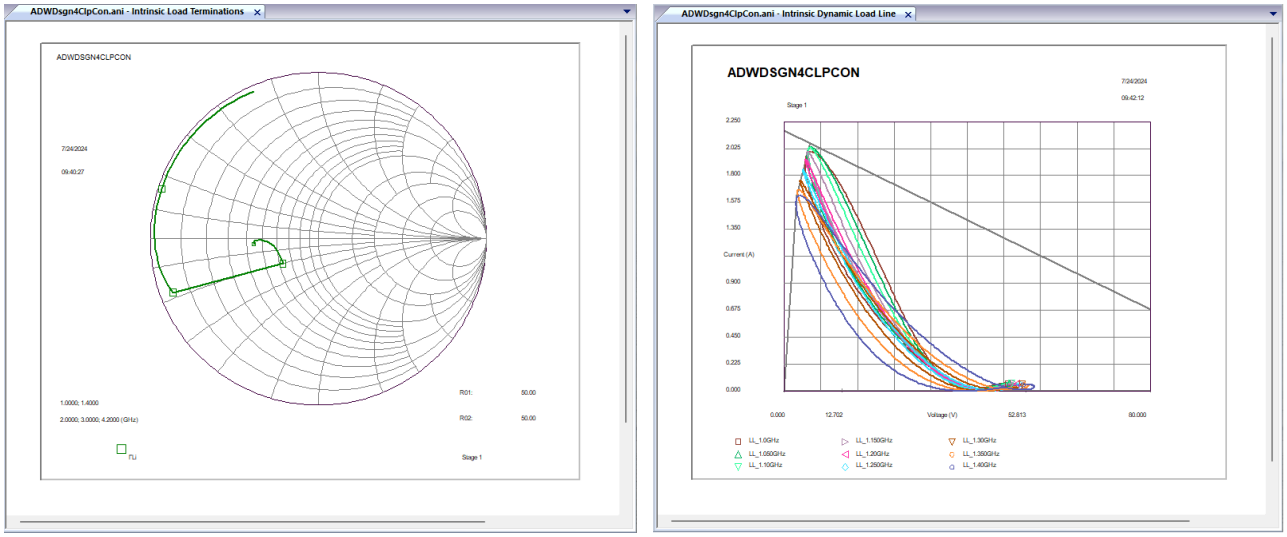

Figure 13. The intrinsic impedances and dynamic load lines associated with the matching network synthesized to solve the clipping contour problem in Figure 12.

With the impedance targets set, matching networks can be designed with the ADW Matching module. Lumped-element, commensurate distributed, non-commensurate distributed and mixed lumped/distributed networks can be designed in the Matching module. The IIM wizard (CMA option) provided in the Analysis module can be used to design phase-controlled matching networks based on T- or PI-sections [10]. The DSLT wizard can be used to design stepped-line transformers for purely resistive matching problems.

The options provided by the DSLT wizard are shown in Figure 14. The ADW schematic element to the left of the insertion point for the transformer to be synthesized must be selected before the DSLT wizard is launched. This is illustrated in Figure 15. The artwork for a stepped Klopfenstein taper [11] is shown in Figure 16 with the gain and the input reflection coefficients. Note the equiripple performance. The insertion loss for the taper is 0.42 dB in the passband (1.0 – 2.75 GHz) and 1.1dB at 13.75 GHz (fifth harmonic). The length of the taper is 69 mm. The electrical length of a Klopfenstein taper is around 180° at the lowest passband frequency. Using a stepped-line taper is generally better than using quarter-wavelength stepped lines (first three options in Figure 14) when two or more stepped sections are required.

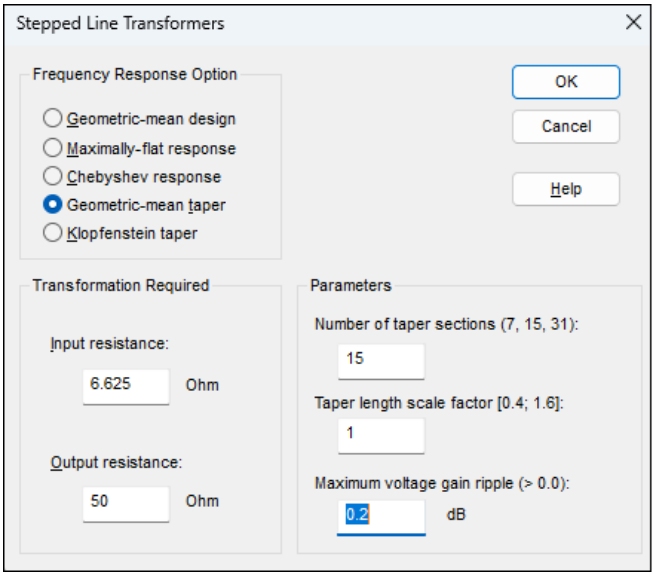

Figure 14. The stepped transformer options provided by the DSLT wizard.

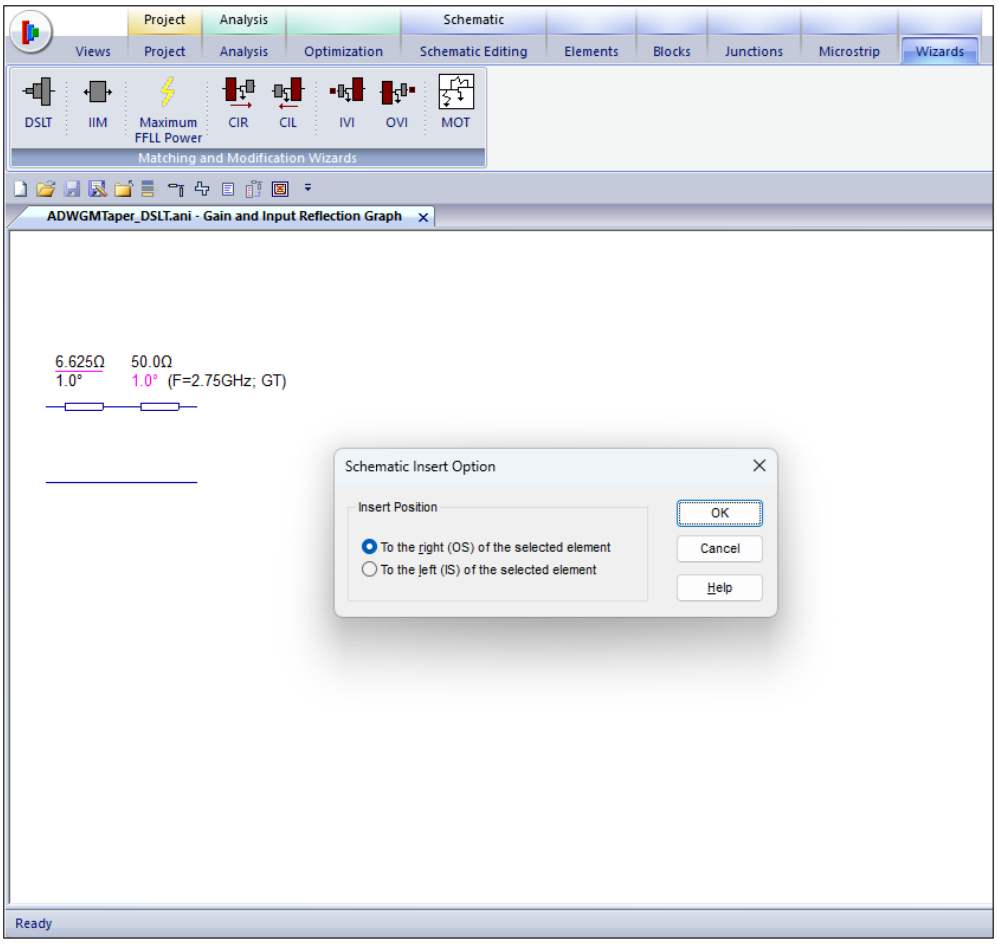

Figure 15. The schematic element to the left of the insertion point for the stepped-line transformer or the matching network to be synthesized must be selected before a wizard is launched.

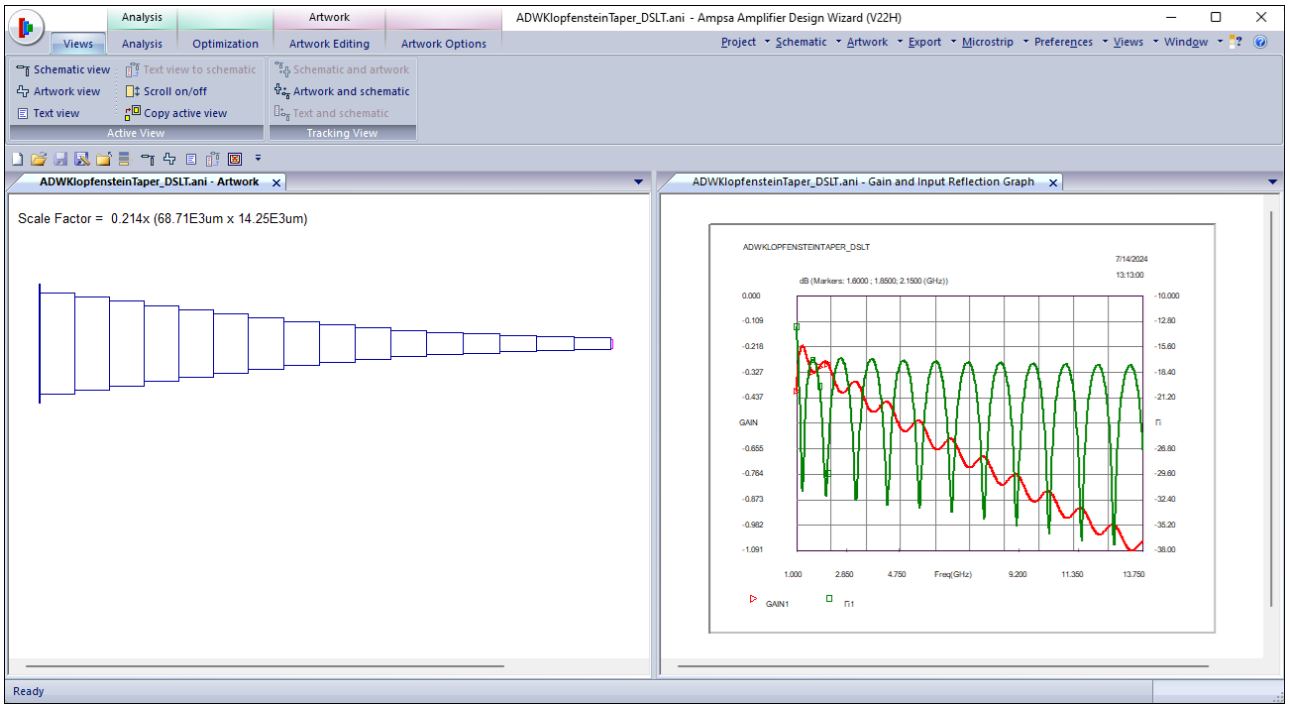

Figure 16. A Klopfenstein [11] stepped-line taper designed by using the DSLT wizard. The gain and the reflection coefficient are also shown here.

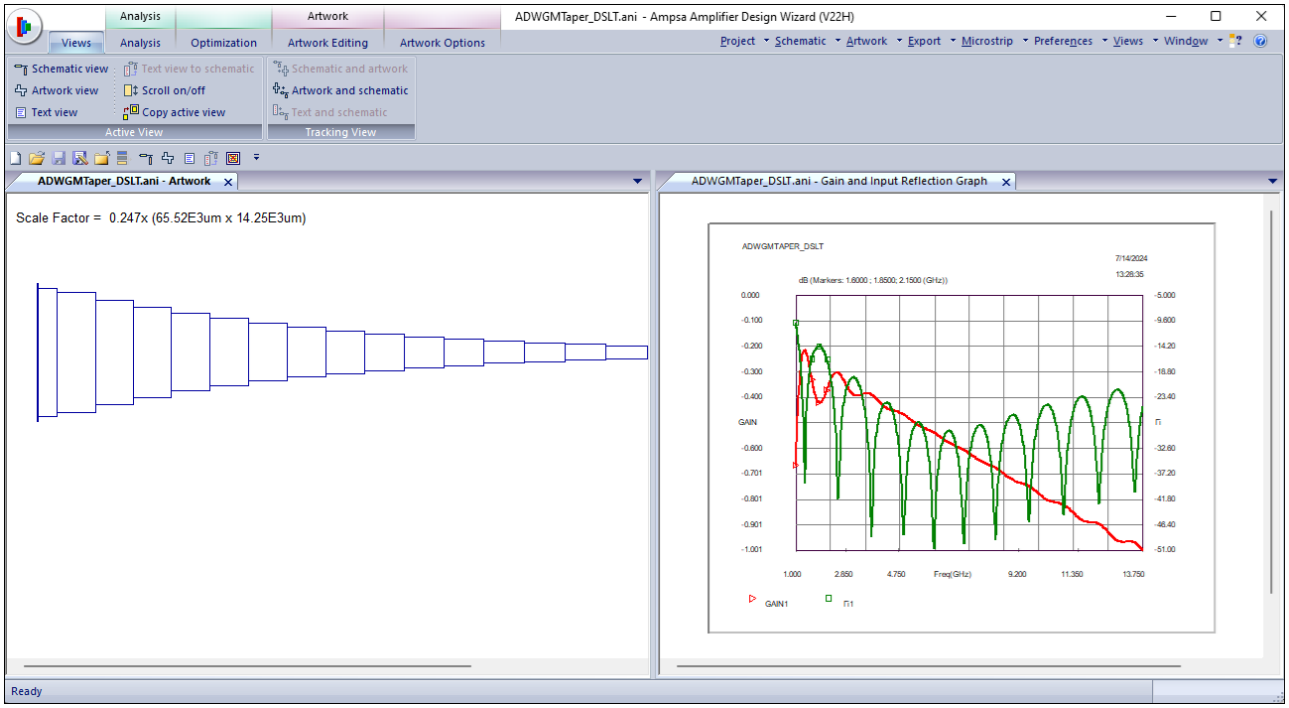

Figure 17. A geometric-mean equivalent for the Klopfenstein stepped-line taper in Figure 16.

The taper can be edited to be continuous by joining the corners of the taper sections. Keeping the transformer in stepped form can, however, be advantageous - The lengths of the stepped lines can be optimized to improve the performance of the circuit in which it is embedded. This includes adjusting the section lengths to reduce the effects of the step discontinuities.

An equivalent geometric mean taper is shown in Figure 17, with the associated gain and reflection coefficients. The length of this taper is 66 mm. The taper length can be increased to improve the performance at the lower frequencies in the passband (Taper Length Scale Factor in Figure 14). The factor by which the length should be increased can be set to the ratio of the first frequency with acceptable performance to the lowest passband frequency. The reference points for this taper are the centres of the segments.

The Matching module is usually used to solve matching problems in the ADW. The synthesis algorithm for non-commensurate distributed networks was extended recently to introduce harmonic traps (transmission zeros) in the synthesized matching networks. The importance of traps in the control of the harmonic performance was illustrated in [12] with a matching network based on an elliptical filter prototype. The results shown in [13] for a 1.0 – 3.8 GHz 10W power amplifier are also impressive.

To provide the extended control, a shunt capacitive branch or a shunt inductive branch in a non-commensurate distributed ADW matching network can now be designed for resonance at the transmission-null (attenuation pole) frequency specified while still providing the reactance required at the fundamental-frequency of interest (See Figure 18). Different trap frequencies can be specified for shorted-stub branches and open-ended stub branches.

The electrical line lengths are fixed in commensurate networks, and the characteristic impedances are the variables. (In the ADW, different lengths can be used for the main-line sections, the open-ended stubs, and the shorted stubs.) The stub lengths can, therefore, be set for trapping. The

characteristic impedance is set to provide the reactance required at the transformation-*Q* frequency. (That is, if the characteristic impedance required is inside the range targeted.)

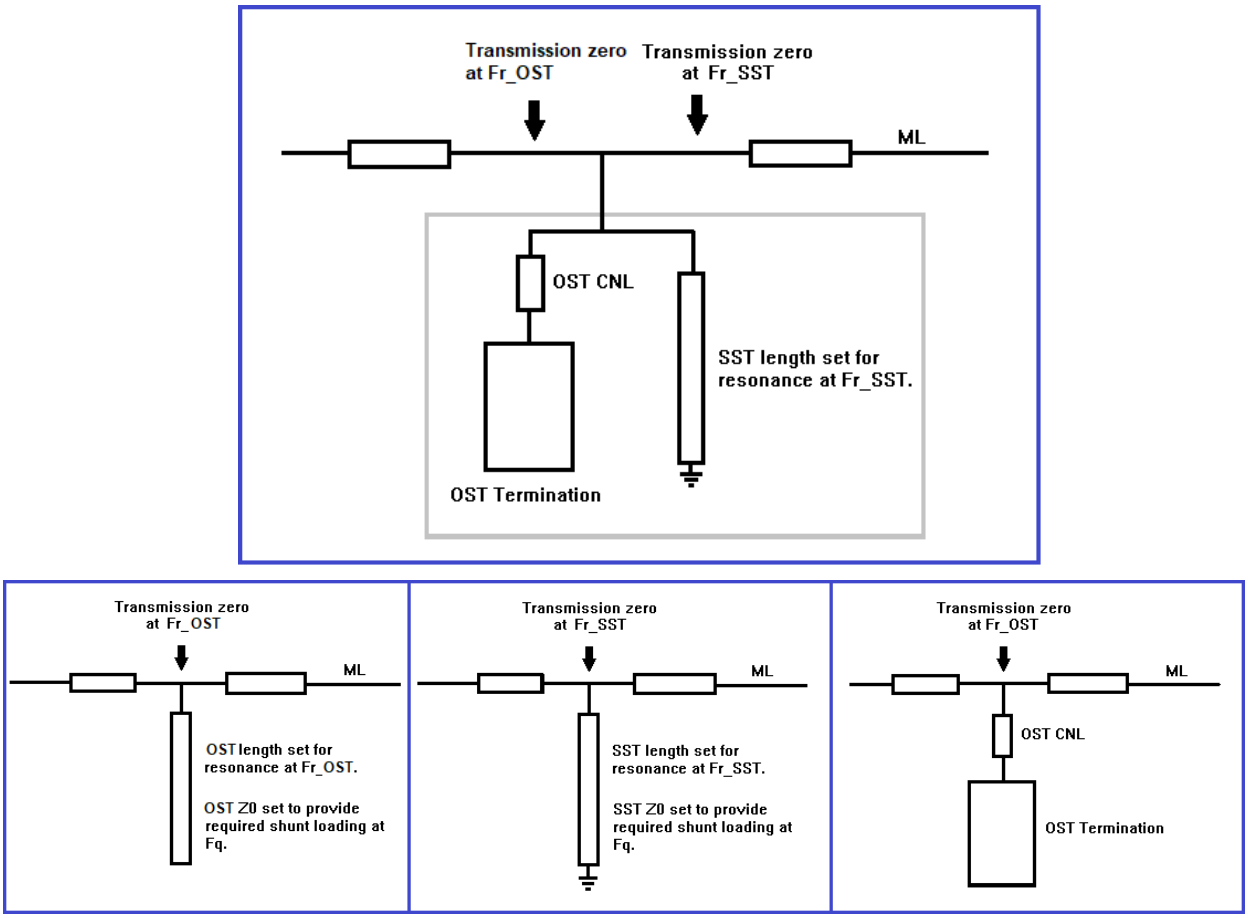

Figure 18. Distributed traps based on shorted and open-ended stubs, respectively. Each of these traps provides resonance at the trap frequency targeted and presents the shunt impedance required at the transformation-*Q* frequency.

The short or open presented by a harmonic trap should ideally be transformed to the intrinsic harmonic load impedance required [13]. A phase-controlled matching network can be designed for this purpose, but a series connected transmission line may suffice. The parameters of the series lines required for several second harmonic and third-harmonic traps are listed in the ADW when the CIL wizard is used.

Ideally, harmonic traps should not affect the terminations at the fundamental frequencies. The loading effect of the traps at the fundamental frequencies are also listed in the ADW. When the loading is light and the line required for transforming the transmission-null impedance to the desired intrinsic load impedance is electrically short, the trap can be added to the circuit before a matching network is designed. However, better results are frequently obtained if the traps are part of the matching network instead.

The impedance-matching targets in the ADW are defined at the insertion point for the matching network. If the CIL wizard was used to setup a load matching problem, the intrinsic harmonic terminations can also be targeted directly (Version 23 and higher).

Multiple solutions are provided to each matching problem and knowing the intrinsic load terminations associated with each solution makes it much easier to select the best solution. This feature was introduced in Version 21 of the ADW.

The intrinsic and external reflection coefficients of a wideband ADW matching network (Passband: 1.0 – 3.9 GHz) are compared in Figure 19. (Note that this is a Version 22 example.) The behaviour is essentially Class-B (with reduced second-harmonic content) over the whole band (1.0 – 11.7 GHz).

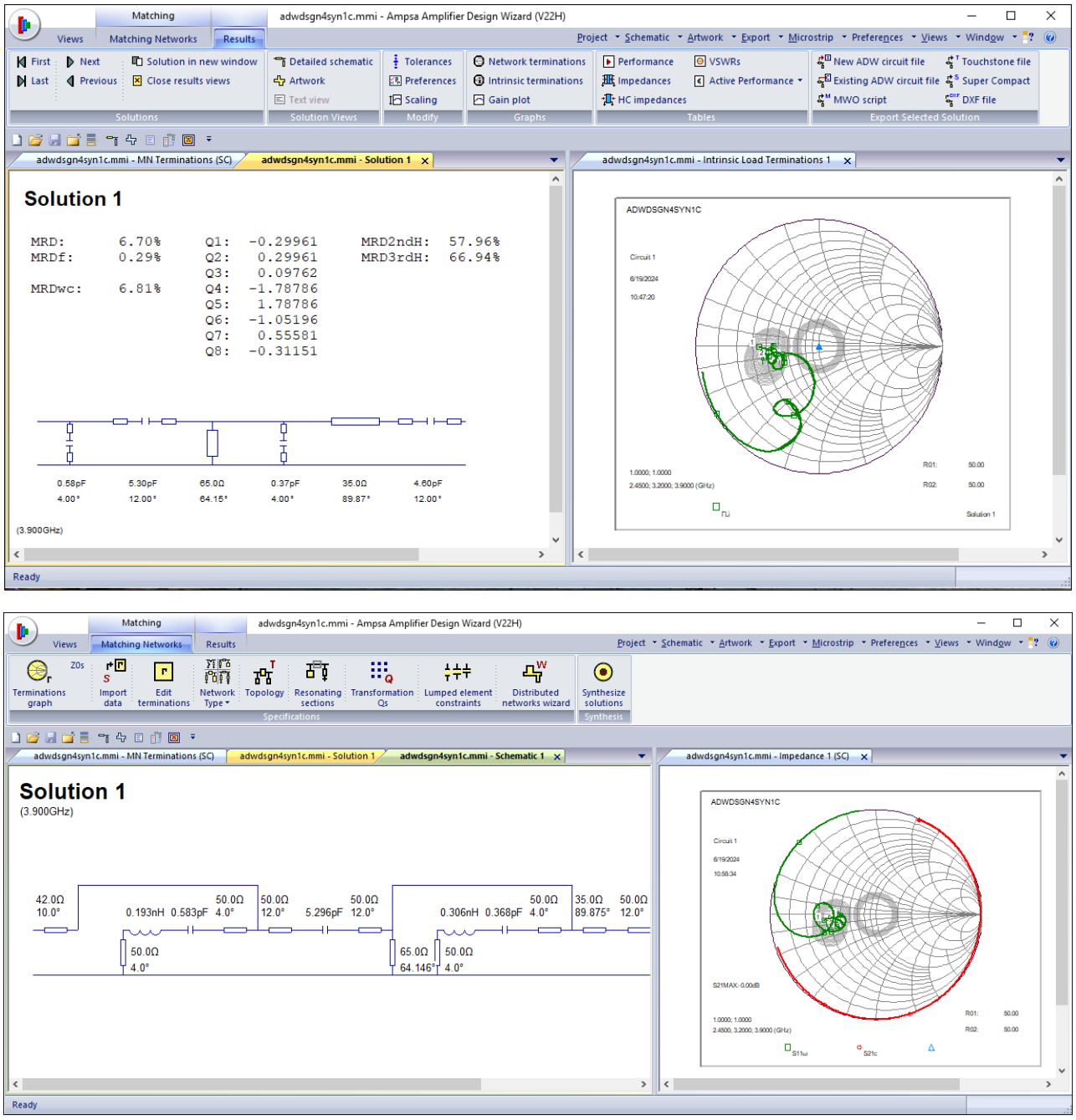

Figure 19. The intrinsic and external reflection coefficients for a wideband matching network are compared here (Passband: 1.0 – 3.9 GHz). The input reflection coefficient traces shown are for 1.0 – 11.7 GHz.

An example of an ADW amplifier with harmonic traps is shown in Figure 20. The intrinsic load reflection coefficients presented to the transistor are also shown.

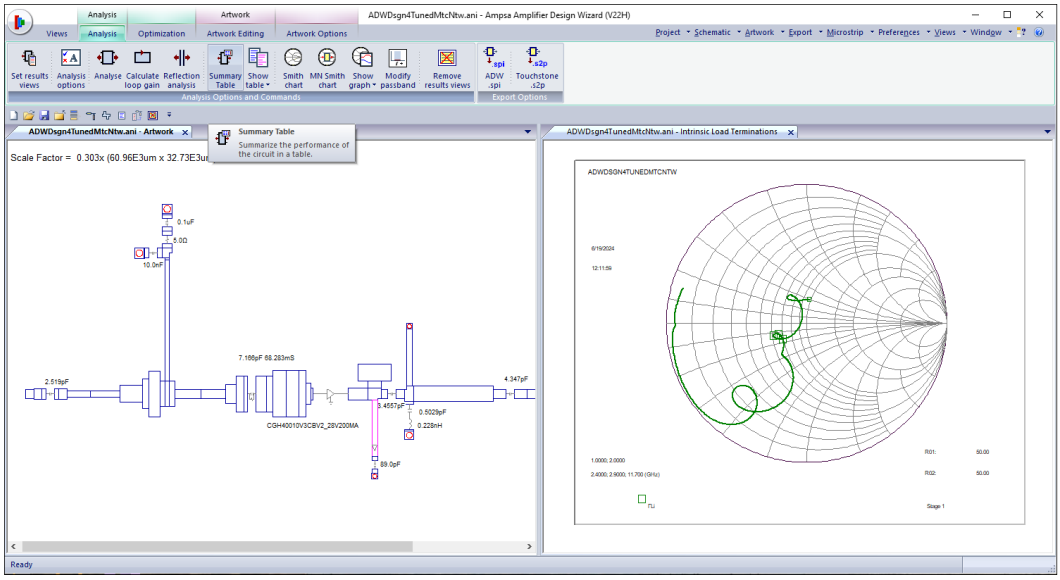

Figure 20. An example of a wideband ADW amplifier with harmonic traps. The passband is 1.0 – 3.9 GHz. The intrinsic load reflection coefficients presented to the transistor by the matching network are also shown here.

The ADW was developed to design impedance-matching networks and single-ended amplifiers. However, many amplifier configurations can be transformed to single-ended equivalents. These include push-pull stages, balanced amplifiers, amplifiers using symmetrical combinations networks (see Figure 21), Doherty configurations (see Figure 22) and some load modulated balanced amplifier (LMBA) configurations.

In the circuit shown in Figure 21 (symmetrical combination networks) Z_{HALF} and Z_{DBL} are ideal transformers used to restore the impedance levels in the equivalent single-stage circuit to those in the original circuit. T-section models are used for the microstrip T-junctions. The transistor voltages and currents in this circuit and in the original circuit are identical. If a driver amplifier is used, the power extracted from the single-stage equivalent, as well as the *dc* current required by it, must be multiplied by a factor four in the example shown. This is required to keep the efficiency calculations in agreement.

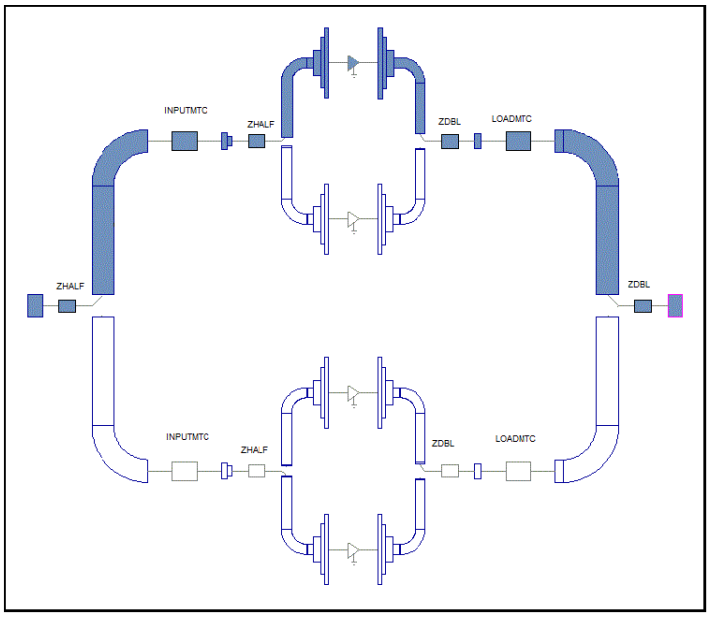

Figure 21. Illustration of the modifications required to simplify the design of a power stage with symmetrical combining networks to a single-ended design.

When a Doherty amplifier is designed, the ratio of the main amplifier current and the peaking amplifier current at the summing node can be used to simplify the design to designing two single-ended amplifiers (see Figure 22). The load matching network for the main amplifier is designed to provide the required output power at two drive levels (peak power and medium power) with maximum or high efficiency targeted at both power levels. The matching network is, therefore, required to solve two different matching problems at the same time. Fortunately, the load terminations for the two problems are different. (Load modulation by the auxiliary amplifier when the power delivered is above the medium power level.) In the ADW, slight offsets in the frequencies of the two matching problems are used to integrate the two problems into one.

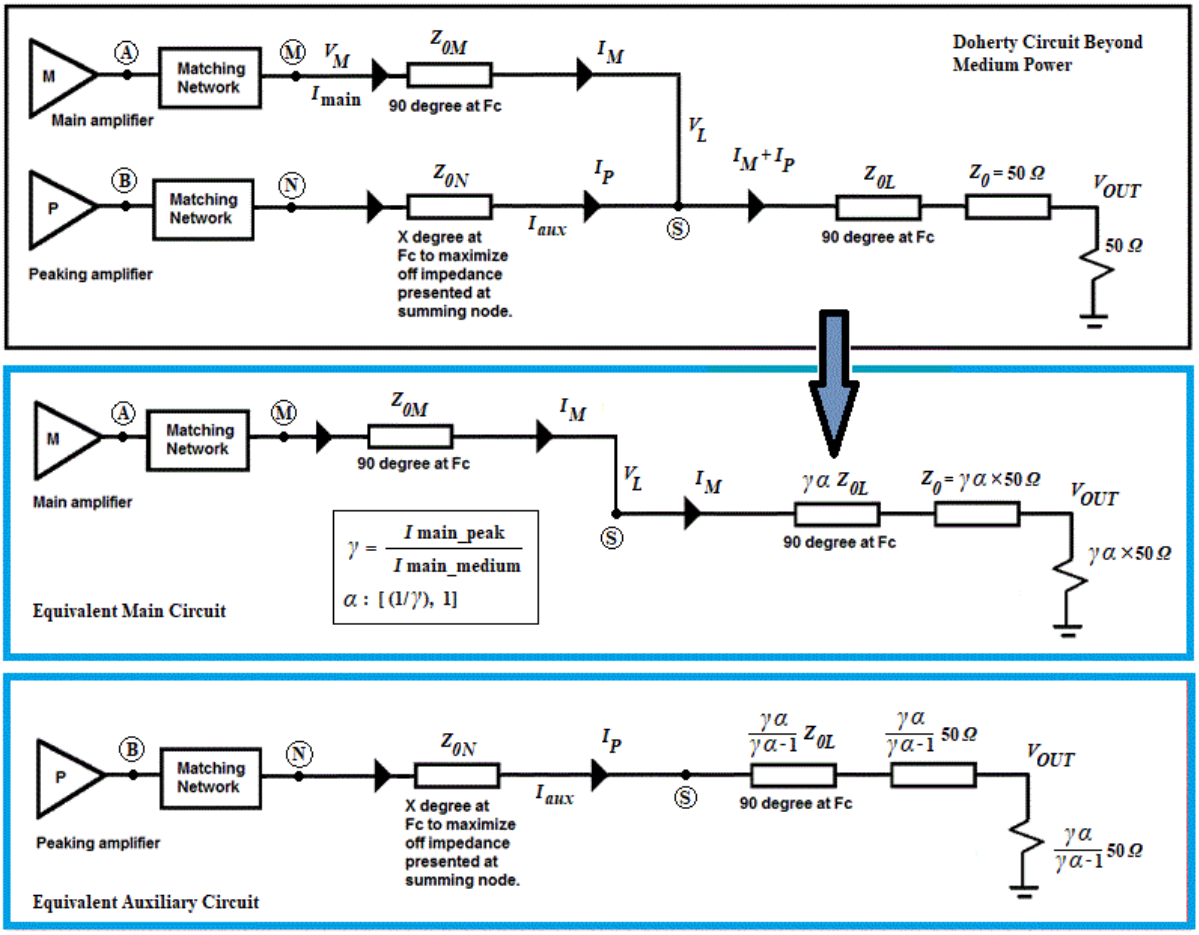

Figure 22. Illustration of the process to simplify the design of a Doherty amplifier to designing two single-ended amplifiers. The matching network for the main amplifier must solve two different matching problems at the same time ($\alpha = 1/\gamma$, as well as $\alpha = 1$).

In linear amplifiers, transistor behaviour is mostly linear up to the point at which a transistor starts to run out of voltage or current. The output power at this point is the maximum unclipped or the hard-clipped output power (P_{muc}). The transistor behaviour will become more non-linear as the transistor is driven (deeper) into compression.

The output power obtained from a transistor is a strong function of the maximum unclipped (or hard clipped) output power. At this power level the intrinsic load line will clip one of the boundary lines specified to define the allowable load-line area for the transistor in the intrinsic *I*/*V*-plane [1]. Up to five boundary lines can be specified in the ADW. (The fifth boundary line is used to approximate the curved upper-left corner of the transistor knee.) Pulsed or *dc* *I*/*V*-curves can be used to define these boundaries. If *I*/*V*-curves are not available, the information provided in the data sheet can be used to

set approximate boundaries. When measured or harmonic-balance results are available, the boundaries used can be adjusted to improve the correlation.

Note that the intrinsic load terminations will be different for different classes of operation. In the ADW, the intrinsic load terminations are mapped to the external terminations by using power parameters [2]. These parameters are derived from the ADW model fitted to the transistor. Under the assumption of linearity, the mapping is exact. The mapping remains valid when feedback is applied to the transistor and when losses are introduced in the transistor model. (Note that the actual output power may be less than the intrinsic power generated.)

The maximum unclipped (hard clipped) output power (P_{muc}) is used with the expected saturated output power (P_{sat}) and an assumed compression curve [3] to estimate the actual output power, as well as the gain compression associated with the input power specified.

A transistor is modelled in the ADW with a set of *S*-parameters (typically class A/B), a linear model (allowance is made for C_{ds} to be non-linear) fitted to these parameters, *I*/*V*-plane boundary lines, the harmonic content specified for the different base modes of operation (Class-A, Class-B, Class-F, inverse Class-F and Class-B2) and a few fitting factors. Up to five harmonics (fundamental included) are allowed in the ADW.

The main fitting factors are the difference between P_{sat} and P_{muc} (P_{su}), and the compression efficiency fitting factor (*CmprEfc*). Typical values for P_{su} are around 3 dBm for Class-B and Class-F and around 0.5dBm to 1.0dBm for inverse class-F. When the output power (P_o) is higher than the maximum unclipped (hard clipped) output power, the *dc* current is assumed to be the *dc* current at the maximum unclipped point scaled by a factor POWER[(P_o/P_{muc}), *CmprEfc*]. Below the maximum unclipped power level, the maximum unclipped *dc* current is scaled by a factor POWER[(P_o/P_{muc}), 0.5]. (Derived from: $P_o = I^2 R = V^2 G$.)

The range allowed for *CmprEfc* is [-0.5; 1.25], with 0.75 the typical value for Class-B and Class-F, and 0.0 the typical value for Class-B2 and inverse Class-F. When *CmprEfc*=1.0, the *dc* current will increase linearly with the power ratio (P_o/P_{muc}). When *CmprEfc*=0.0, the *dc* current will not change, and when *CmprEfc* < 0.0, the *dc* current will be lower than the *dc* current at the maximum unclipped power level.

The load-line boundaries, the harmonic content and the fitting factors can be modified to improve the fit with measurements, or the results obtained in a harmonic-balance simulation.

The output driving waveform in a Class-B or a Class-F amplifier stage is the intrinsic output current, while the intrinsic output voltage is the output driving waveform in an inverse Class-F or a Class-B2 stage. The driving waveform is usually taken to be an ideal or an approximate half-sinusoid. The better option is usually to use the approximate half-sinusoid (limited to *dc*, fundamental-frequency, and second-harmonic components). The results obtained by assuming a perfect half-sinusoid are usually optimistic.

With ideal load terminations, third-harmonic wave-shaping components in the output response waveform do not affect the output driving waveform. However, with non-ideal third-harmonic terminations and assuming linearity, a third-harmonic component is required in the driving waveform to create the third-harmonic component in the response waveform. (This also applies to higher harmonics.) It follows that the driving waveform will then be distorted by any components generated in the response waveform. (The distortion will be associated with a reduction in the component causing the distortion.) In the ADW, the distortion can be ignored or can be clipped to a specified

level (typically 1% of the fundamental-frequency output driving waveform current or voltage). The distortion is limited by clipping the harmonic content generated. Note that some of the wave-shaping components can originate in the nonlinear capacitors instead of the output driving waveform.

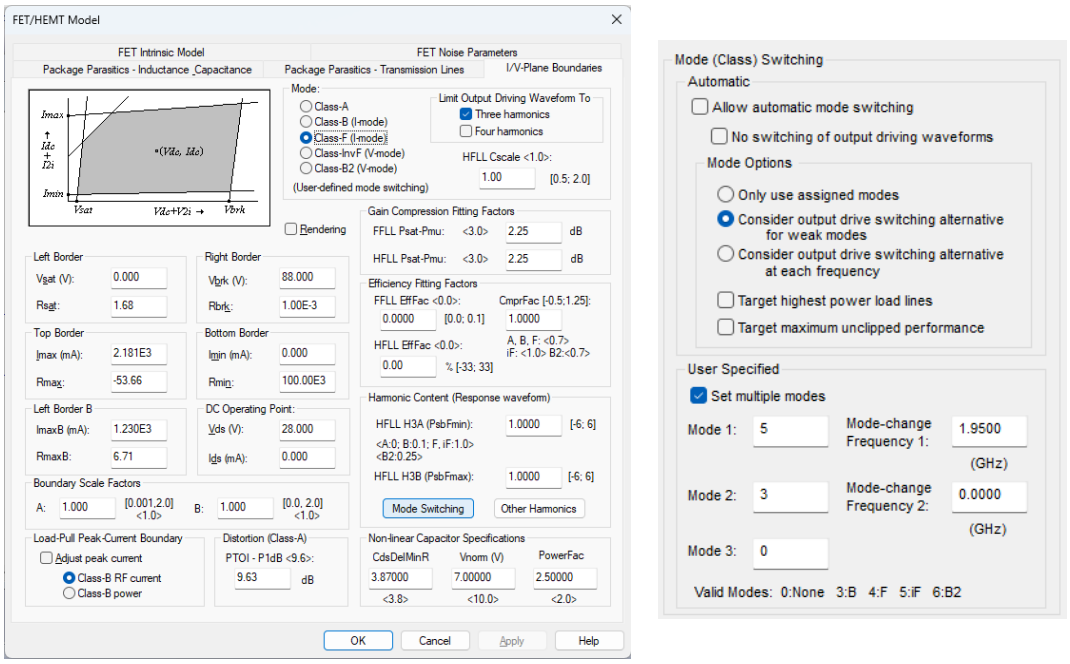

Figure 23. The mode-switching options provided in the ADW. Use the Project | Transistor Models Used ribbon command provided in the Analysis module to open this wizard.

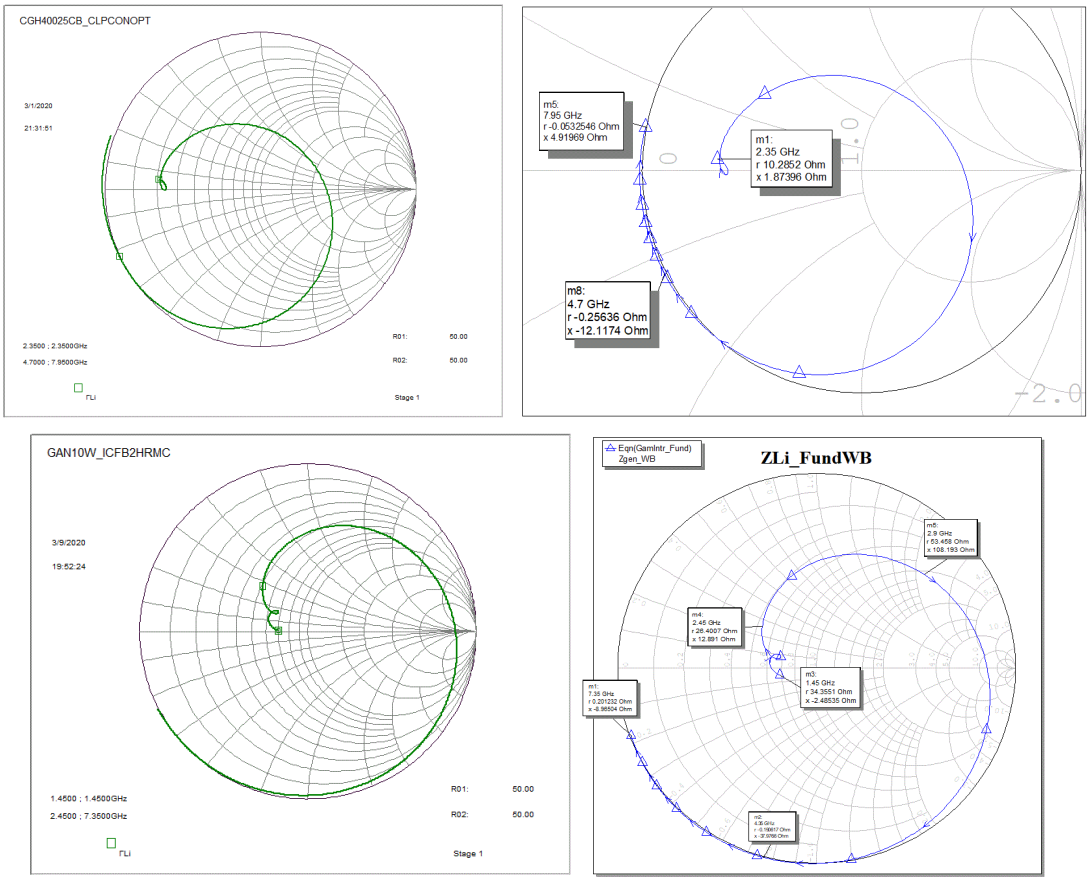

Figure 24. The intrinsic load reflection coefficients presented by two ADW matching networks are compared with the reflection coefficients calculated in Microwave Office™.

The mode of operation in an ADW circuit can be assumed to be fixed at all the frequencies of interest (passband), or mode switching can be allowed (See Figure 23). When mode switching is allowed, the intrinsic impedance presented to the transistor at the frequency of interest can be used to automatically assign a mode of operation at that frequency. When the intrinsic load terminations do not point to any specific mode (strongly resistive harmonic terminations or strongly reactive intrinsic terminations which are not balanced by continuous-mode operation) class-B operation is assumed in the ADW. Options to use the mode which will yield the highest power or the highest efficiency with the assumed harmonic content for the mode considered are also provided (refer to Figure 23).

Allowance is also made for user-defined mode-switching (see Figure 23). Up to two mode-switching frequencies can be specified (three modes). The fitting factors used for the different modes should be adjusted for smooth transitions at the transition frequencies.

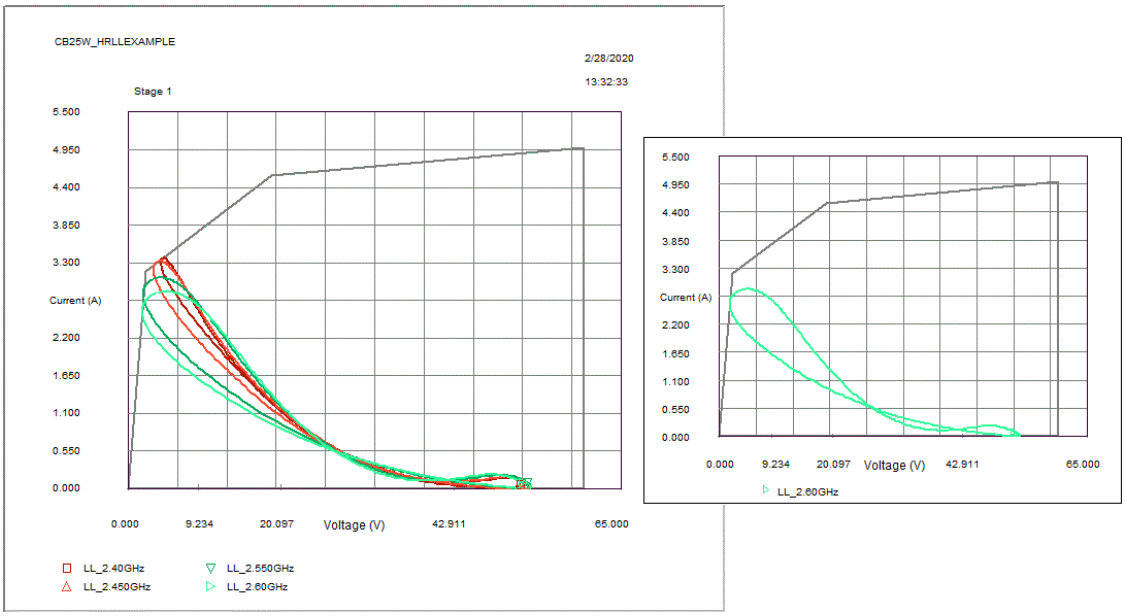

Figure 25. ADW dynamic load lines constrained by five boundary lines.

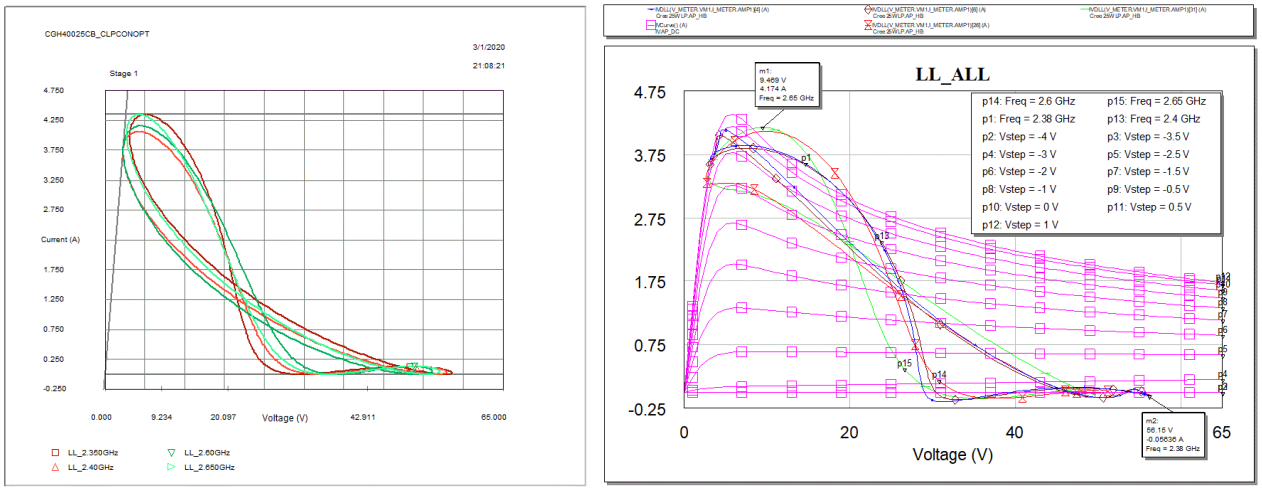

Figure 26. ADW dynamic load lines are compared with the harmonic-balance load lines generated in Microwave Office™. The power levels for the ADW load lines are the maximum unclipped (hard clipped) output power (P_{muc}). The power levels for the Microwave Office™ load lines are closer to the saturated power levels (Interaction with the boundaries; compression).

When an ADW circuit is analyzed or tuned, the intrinsic load reflection coefficients and the dynamic load-lines, as well as the intrinsic output voltage and current can be displayed graphically (see Figures 24 – 26). Five boundary lines were used in the example shown in Figure 25, while four lines were used in Figure 26. The Microwave Office^{TM} load-lines for the Figure 26 example are also shown in Figure 26.

Note that the intrinsic load terminations can also be optimized when the power performance is optimized. The intrinsic load terminations calculated in the ADW generally correlates very well with the terminations obtained in a harmonic-balance simulation (See Figure 24).

The dynamic load lines for a Class-B stage, a Class-F stage and an inverse Class-F stage are shown in Figure 27. The load lines were obtained by optimizing the power performance in each of the associated circuits. The circuits were setup to control the intrinsic load impedances presented to the transistor at the fundamental-frequencies and at the second and third harmonics, independently (load-pull).

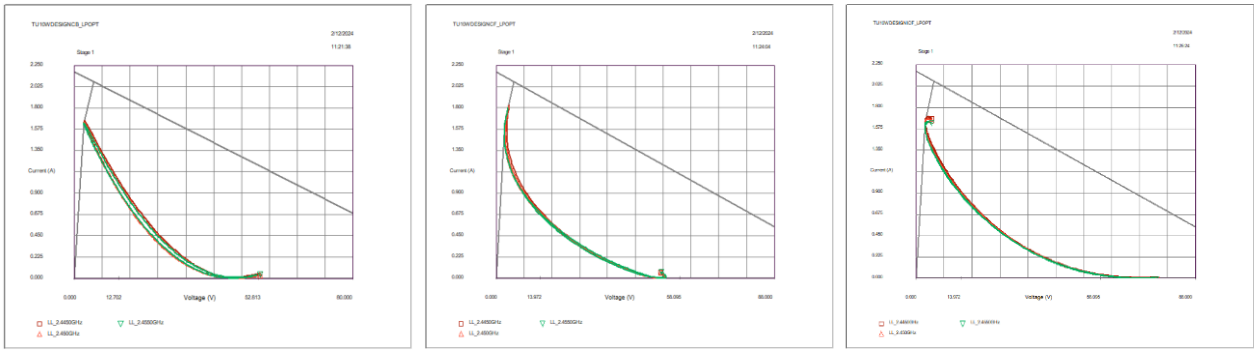

Figure 27. ADW dynamic load lines for Class-B, Class-F, and inverse Class-F modes.

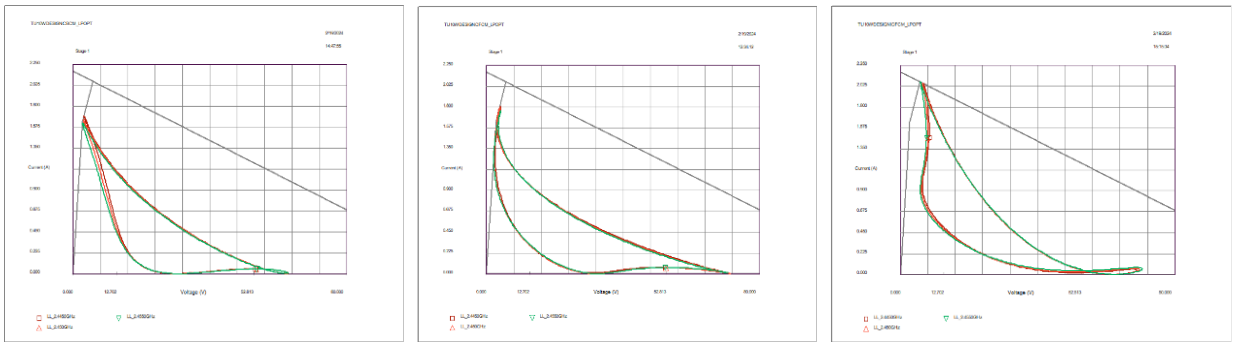

Figure 28. ADW dynamic load lines for continuous Class-B, Class-F, and inverse Class-F modes.

Continuous-mode operation is allowed in the ADW (continuous Class-B, Class-F, and inverse Class-F). The continuous-mode phenomenon is essentially a linear process in which the detrimental effect of fundamental-frequency reactance or susceptance on the power and the efficiency is cancelled by second-harmonic reactance or susceptance of the opposite sign and the correct magnitude. Full cancellation is only possible up to a specific fundamental-frequency Q-value (X_{Li}/R_{Li} ratio) for the mode considered, but the detrimental effect can still be reduced for higher Q-values. The same power and efficiency can, however, not be maintained when the Q-value is out of range.

The dynamic load lines for continuous versions of the Figure 27 stages are shown in Figure 28. The Q-factors for the fundamental-frequencies impedances were around 0.5. Note the higher voltage swings for the continuous Class-B and continuous Class-F modes. (The maximum currents did not change significantly.) The output power and the efficiency for the base-class and the continuous-mode versions of the Class-B and the Class-F stages are the same.

Note that the peak intrinsic voltage or the peak intrinsic current associated with continuous-mode operation is higher than that associated with base-class operation. The peak voltage is higher for continuous Class-B and continuous Class-F operation, while the current is higher for continuous inverse Class-F. When the current is increased, the transistor knee will reduce the benefits of continuous-mode operation (see Figures 27 and 28).

Because of the knee, the performance of the inverse Class-F stage is degraded with continuous mode operation (higher current). The curvature in the knee aggravates the degrading effect.

Note that the slopes in the maximum current boundaries could have been reduced in these examples, but the downward sloping boundaries are useful for avoiding higher power dissipation areas.

The circuits used to create the graphs in Figure 27 are also useful when an ADW model is fitted to a transistor. The performance in the ADW can be compared to measurements or the performance obtained in a harmonic-balance simulation, and corrections can then be made to the ADW model to improve the correlation.

When a model has been fitted to the transistor, the Figure 27 circuits can also be used to establish the range of intrinsic or external harmonic reflection coefficients over which the performance targeted can be achieved (load-pull). Note that when power contours and efficiency lines are generated with the CIL wizard, the harmonics are assumed to be the ideal harmonics for the class of operation assumed. However, the base-class performance sets the upper limit for continuous-mode operation too and the continuous-mode terminations can be obtained by adjusting the base-class terminations appropriately. The price to pay is an increase in the intrinsic output voltage or current, with additional penalties by the transistor knee if the current is increased (see Figure 28). An increase in the voltage can also be a problem if the breakdown voltage of the transistor is not high enough.

The circuit shown in Figure 29 was used to find the optimum Class-F harmonic terminations for the transistor used. The transformers shown are used to control the harmonic terminations presented to the transistor. The transformer on the load side transforms the load impedance of the circuit to the required level inside the passband and presents an open to the left of the insertion point in the circuit outside the passband. The centre transformer performs similarly for the second harmonic – It presents a shunt open outside the second-harmonic band and the stub impedance inside the second-harmonic band. The transformer on the left sets the third-harmonic terminations. The lossless series LC resonator to the left of the fundamental-frequency transformer controls the external fundamental-frequency reactance presented to the transistor.

Note the sliders provided in the summary tables shown in Figure 29. The value of the element selected in the schematic when the summary table is opened (Analysis | Summary Table ribbon command) can be tuned with the slider. The element selected must be set for optimization (Optimization | Optimize Element ribbon command). Any optimization bounds set for the variable will be used but can be overridden by the tuner (Close the summary table when a limit has been reached and re-open it - the tuning range will be adjusted automatically).

One would expect that tuning the external resistance would have a strong effect on the intrinsic load resistance (and similarly for the reactance). However, in this circuit and at the frequency of interest, the external resistance has a strong effect on the intrinsic load reactance, while the external reactance has a strong effect on the intrinsic load resistance. The reason for this can be deduced from Figure 19.

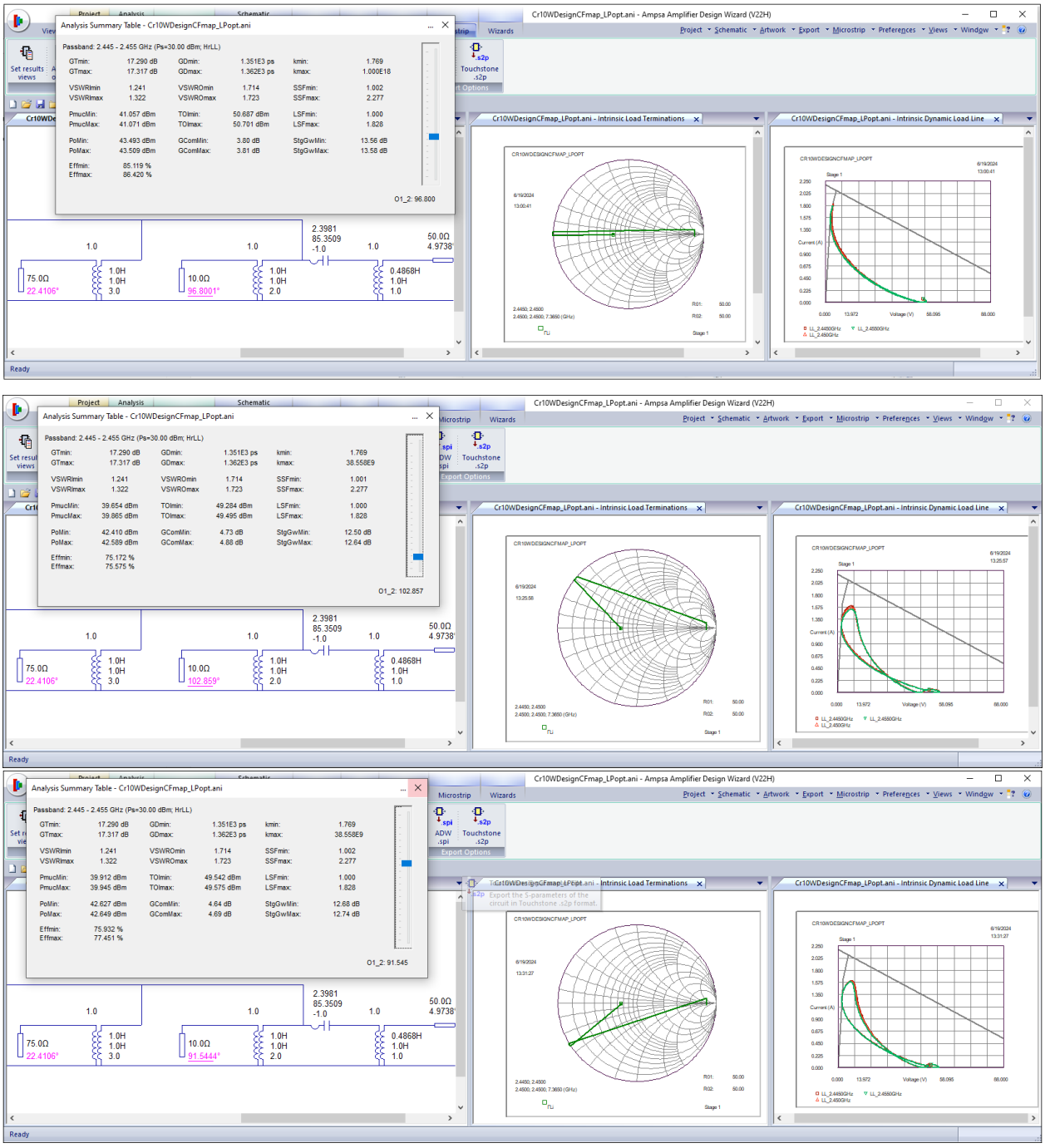

Figure 29. The range of purely reactive intrinsic second-harmonic reflection coefficients over which the efficiency for the Class-F stage in Figure 27 will be above 75%.

The circuit shown in Figure 29 was first optimized for optimum Class-F performance (P_o=43.5dBm, η=85%). The second-harmonic termination was then tuned up and down to the 75% efficiency points with the optimum fundamental-frequency and third-harmonic terminations in place. Finally, the effect of the third-harmonic termination was established at each of the three second-harmonic points. The third-harmonic effect was not severe - The efficiency obtained was higher than 72% for all third-harmonic terminations. (Only lossless external harmonic terminations were considered here, but losses can be added, if necessary.) As to be expected, the worst performance was associated with the second-harmonic terminations at the 75% points. The efficiency remained above 76% with the optimum fundamental-frequency and second-harmonic terminations in place.

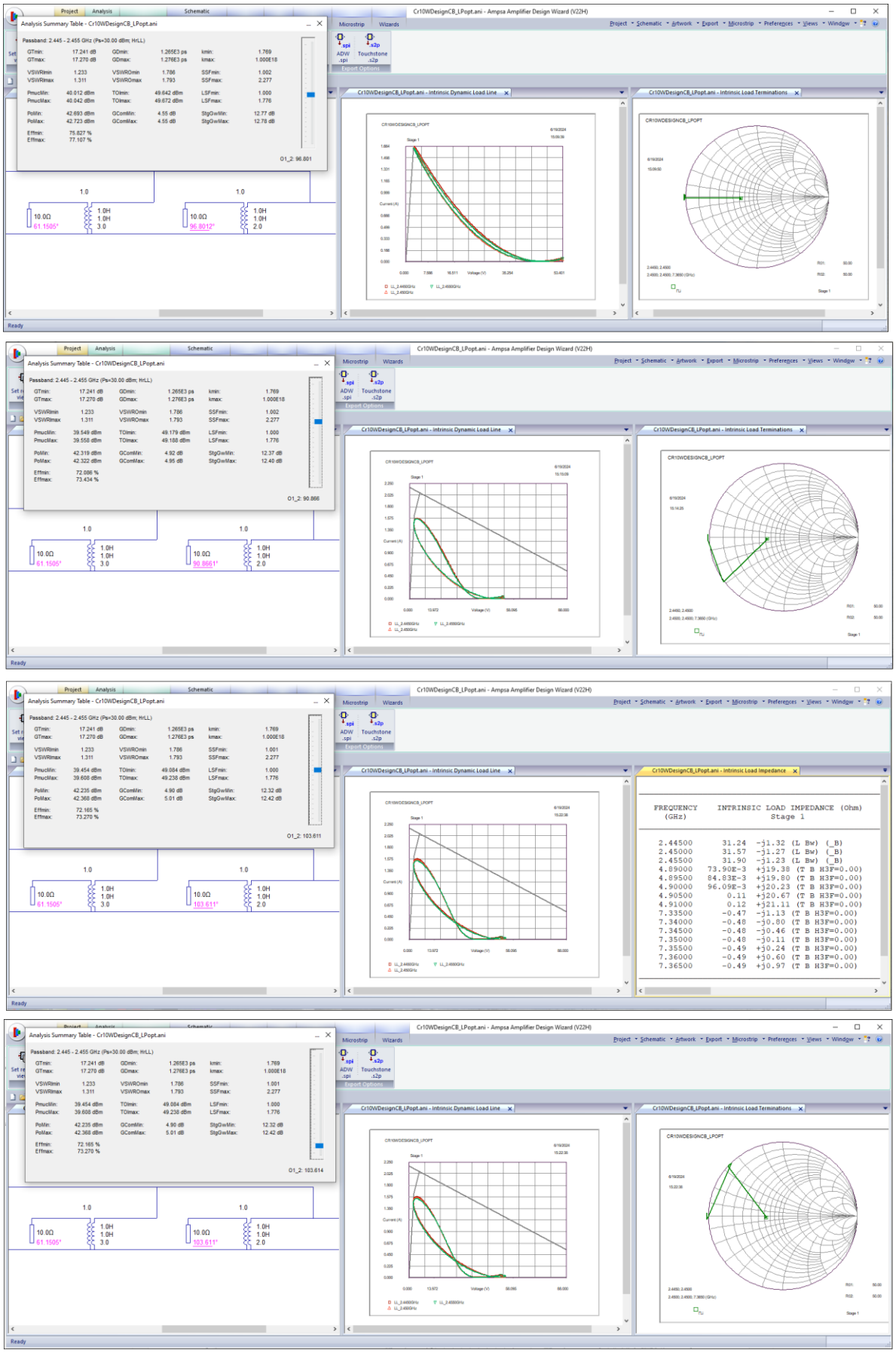

Figure 30. The tuning features in the ADW were used to find the range of second-harmonic reactance values to be targeted for Class-B operation in this example.

When the external terminations are tuned, the rate at which the intrinsic reflection coefficients change can be very high over sections of the tuning range (high Q). Because of this sensitivity it would be advisable to avoid these sections when possible. (Scale the optimization range down to counteract the sensitivity.)

A second example of using the tuning features in the ADW to find the range of second-harmonic reactance values to be targeted with a selected fundamental-frequency load is provided in Figure 30. The class of operation in this example is Class-B.

The intrinsic load impedances presented to the transistors are the focal point in a typical ADW design. This also applies when load matching networks are synthesized for an amplifier stage in the Impedance-Matching module. (See Figure 19 for an example.) Knowing the intrinsic load terminations associated with a matching network makes it easier to decide on the best solution to the problem. The error function used to decide the best solutions to a matching problem can also target the intrinsic harmonic terminations directly if the matching problem was setup by using the CIL wizard. This capability was introduced in Version 23.

If the intrinsic harmonic terminations are too far off-target, the mode of operation may not be the mode targeted when the impedance-matching targets were set.

Note the anticlockwise rotation from external to intrinsic in Figure 19, as well as the tighter bundling of the intrinsic reflection coefficients. At the lower passband frequencies, the harmonic terminations in this example are highly resistive (the harmonic bands and the passband overlap) and the assumed mode is then Class-B with reduced second-harmonic current content. At the higher frequencies in the passband the mode tends to be closer to ideal Class-B.

ADW matching networks are usually designed with targets set up under the assumption of linearity. (The circuits associated with Figure 27 could also be used to define targets with C_{ds} nonlinear.) In the final stages of an ADW design, C_{ds} should be set to be non-linear, and the linear and non-linear performances of the circuit should be compared. If necessary, the circuit can be optimized to improve the non-linear performance.

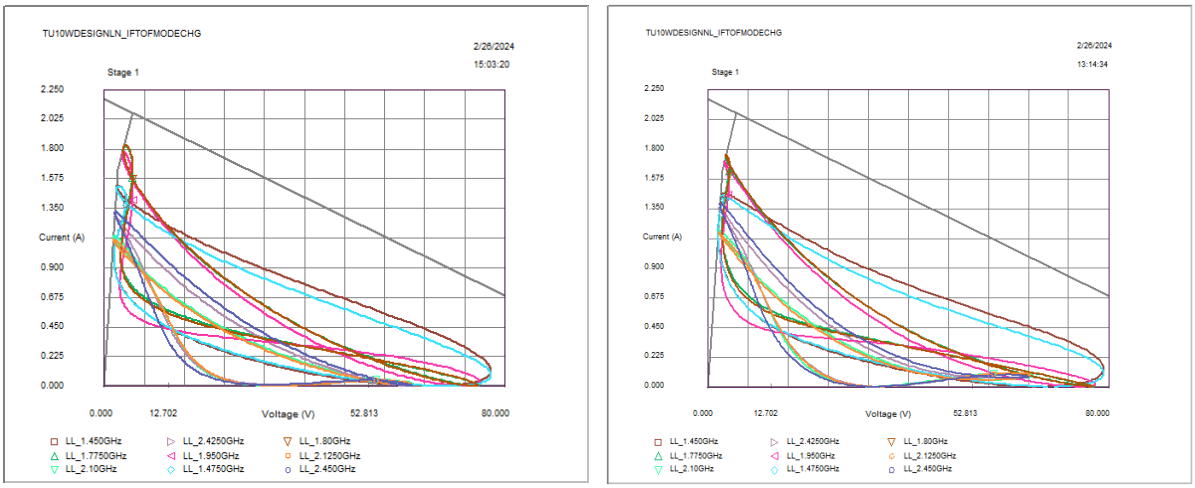

Figure 31. The linear and nonlinear intrinsic load lines for the circuit designed in [5] are compared here.

The coefficients for a typical C_{ds} profile can be specified for each transistor in an ADW circuit. This profile is used when the Assume Linearity Project option is unclicked (Project | Options ribbon command in the Analysis module). Fourier analysis is used to calculate the currents associated with

the C_{ds} voltage waveform. The currents are calculated at the maximum unclipped (hard clipped) power level.

The linear and non-linear intrinsic dynamic load lines for the first single-stage amplifier shown in [5] are compared in Figure 31. Note that the nonlinear load lines are closer to the knee and that the maximum voltages are also slightly higher. The power level for these dynamic load lines is the maximum unclipped output power.

When a matching network is designed, the discontinuities in the design and the parasitic elements associated with the lumped-element components could move the impedances presented by the matching network off-target. It is, therefore, important to keep the discontinuities and the parasitic elements in mind when a matching network is designed.

Implicit or explicit microstrip junctions can be used in the ADW. Implicit junctions do not affect the ADW circuit performance but will affect the dimensions of the lines in the artwork created for the electrical circuit. Note that the electrical circuit (schematic) is simulated in the ADW and not the artwork. When the artwork is created, the geometrical lengths of the lines associated with implicit junctions are adjusted automatically by using the information available in Hammerstad microstrip models [14]. The transformer and loading effects in the Hammerstad T-junction model are ignored when these adjustments are made.

The performance of the ADW artwork will not be identical to that of the electrical circuit (schematic) and adjustments may be required in the artwork or the ADW models used to improve the correlation. Scale factors are used in the ADW discontinuity models to allow for optimization of these models. EM simulation of a junction is required to set the targets for the optimization.

An ADW circuit with implicit junctions can be transformed automatically to have explicit junctions by using the Artwork | Export Options | Convert Implicit Junctions ribbon command. Hammerstad [14], Gopinath [15] or *S*-parameter based junctions can be used in the exported circuit. *S*-parameter based step, curve, bend, T-junction, and cross junction commands are provided in the ADW.

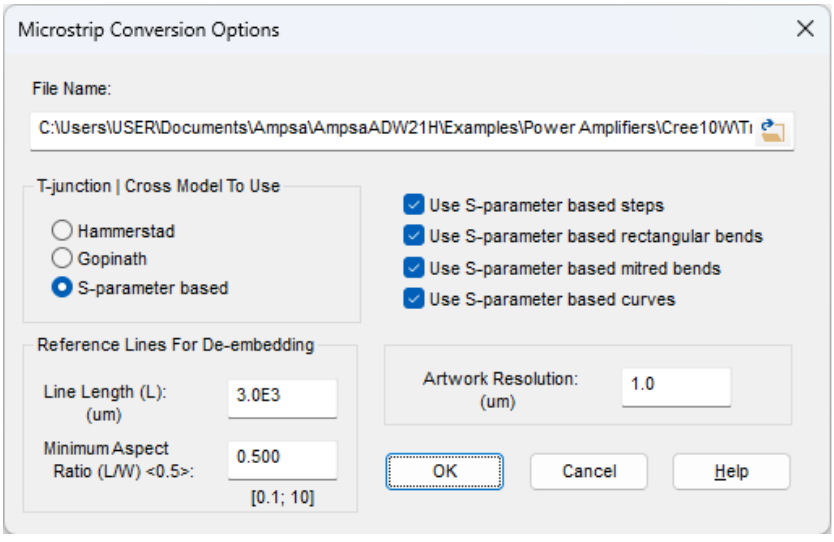

Figure 32. The microstrip options provided when an ADW circuit with implicit junctions is converted to have explicit junctions.

When the *S*-parameter based export option has been selected (see Figure 32), ADW circuit files (.ani) will be created automatically in the Export Folder for all the discontinuities (steps, rectangular bends,

mitred rectangular bends, curves, T-junctions, and crosses) in the circuit. These files can be used to export the artwork required for the EM simulations (.son, .dxf or .bas files). The file names are set to make the process efficient. The root part of the name assigned to the *S*-parameter file exported from the EM simulator (.s2p, .s3p or .s4) should be the same as the name of the file created by the ADW. The ADW is setup to extract the junction information from the assigned name when the EM *S*-parameters for a junction are imported (Schematic | Junctions | Import *S*-parameters ribbon command).

Note that it is very easy to change the substrate in the ADW when explicit junctions are not used. It is, therefore, advisable to delay using explicit junctions until it has been established that the substrate chosen is a good choice for the circuit designed.

The best way to minimize EM issues with circuits designed in the ADW is to replace the implicit or standard junctions in the final ADW design with *S*-parameters based junctions. (It is also necessary to allow sufficient spacing between the different junctions.) With the junctions sorted out, the ADW network can then be optimized to restore the performance before it is exported for EM (and harmonic-balance) simulation and optimization.

Reverse optimization may also be an option for adjusting the ADW artwork. Each matching network designed in the ADW is then analyzed in an EM simulator and the EM *S*-parameters are used as targets to optimize the ADW network. When the ADW circuit components are updated after the optimization, the changes to be made to the circuit are then applied in reverse (that is, if a line is required to be longer, it is made shorter instead). The performance of the modified artwork in the EM simulator will generally be closer to the performance of the original ADW schematic.

Choosing a suitable substrate and constraining the characteristic impedances adequately are important when a matching network is designed, especially when harmonic control is also required. EM simulations provide the feedback to select a better substrate and to tighten or reduce the constraints on the characteristic impedances. Using thick metal in the EM simulations is advisable and care should also be taken with the loss factor used for the substrate. (The loss factor could increase significantly with increasing frequency.) Box resonances in the harmonic bands of interest should also be avoided. Using the free space option for the cover could suppress box resonances. Another option could be to use absorber material.

Ideally, the ADW should be used with Microwave Office™ (MWO) or ADS™. ADW networks (electrical or microstrip) can be exported to MWO via basic scripts (.bas), so this is the recommended option. ADS users can import the ADW artwork into Momentum™ via DXF, while *S*-parameter equivalents for the matching networks can be used to verify the electrical performance obtained in the ADW. The ADW can also create Sonnet® files (.son) for the artwork. The Sonnet files created also provide another path into ADS or MWO.

An ADW circuit can be exported to Microwave Office™ in distributed or in microstrip form. It is advisable to export the distributed (electrical) ADW circuit first. Adjustments in the ADW transistor models may be required and if so, the difference between the discontinuity models used will cloud the process. The harmonic content assumed in the ADW may also differ from the harmonic content in the harmonic-balance simulation. The difference will generally be small if the intrinsic load terminations of the circuit designed in the ADW are well-behaved.

Note that the harmonic content specified for a transistor in the ADW can be optimized to provide a closer fit to the measured or the harmonic-balance performance. This option is provided when the

Optimization wizard is launched (See Figure 33). Note that the Output Power option must be selected when the harmonic content is optimized.

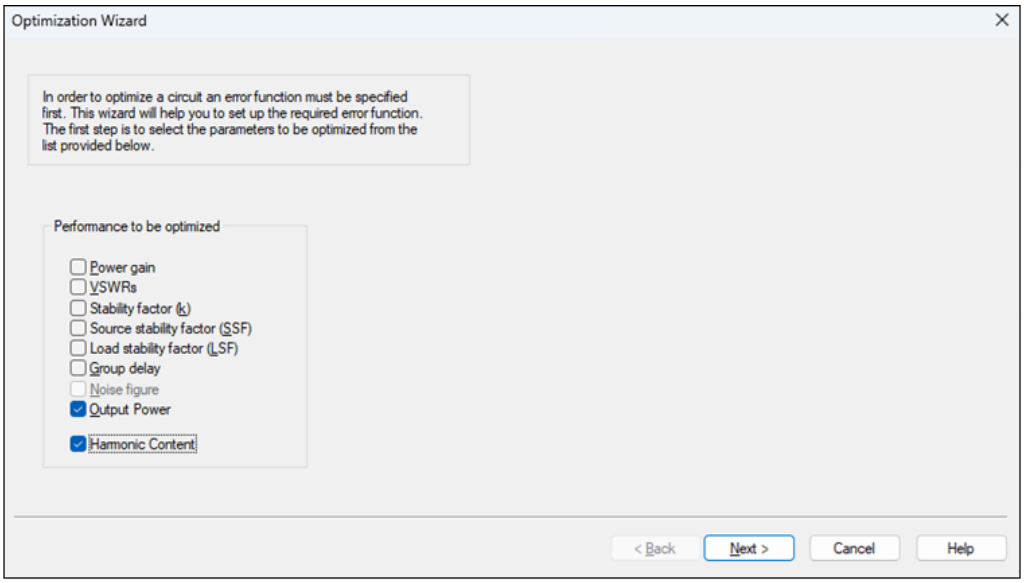

Figure 33. The option to optimize the harmonic content instead of the circuit is provided when the optimization wizard is launched.

When a microstrip circuit has been exported to Microwave Office™ or ADS™, it is good practice to first optimize each matching network to have the same *S*-parameters as in the ADW. This is usually not required when *S*-parameter based commands were used for the discontinuities in the ADW circuit. When optimization or tuning is required, good results can usually be obtained by optimising or tuning the lengths of the lines associated with the discontinuities (differences in the reference planes). When the lines associated with T-junctions or cross junctions are optimized, the stub lengths are usually more important than the lengths of the main-line sections.

Select the ADW Artwork | Artwork Options | Artwork Options ribbon command to set the option to use X-models when an ADW circuit is exported to Microwave Office™.

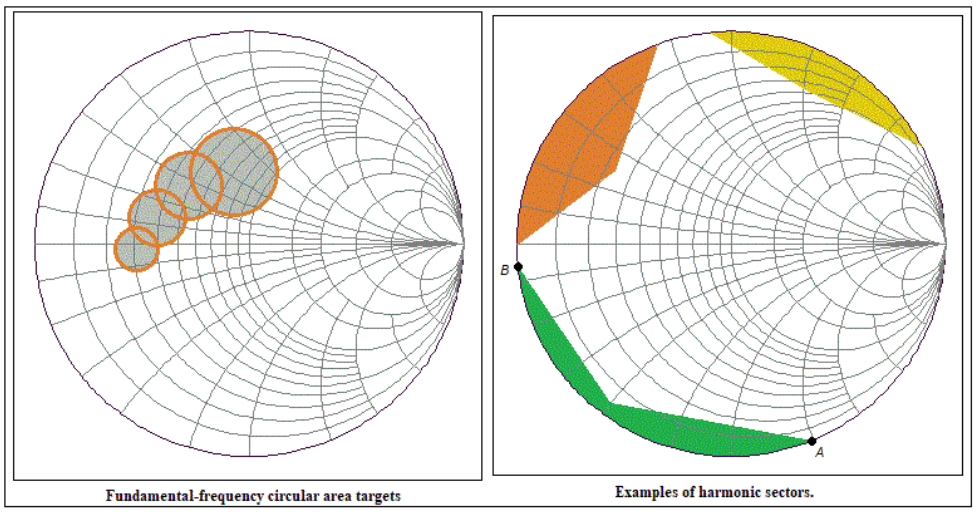

Figure 34. Circular fundamental-frequency areas and Smith chart sectors (harmonic sectors) can be targeted in the ADW impedance-matching module.

Synthesis of impedance-matching networks in the ADW is based on systematic searches on the transformation-*Q*s of the matching networks [2].

When commensurate networks are synthesized, the electrical line lengths are specified by the user and the characteristic impedances are the variables. When non-commensurate networks are synthesized, the characteristic impedances are specified by the user and the line lengths are the variables. A systematic search can be done to find the optimum main-line line length when commensurate networks are synthesized, or the optimum main-line characteristic impedance when non-commensurate networks are synthesized. This eliminates the manual experimentation required previously.

When a matching network is synthesized, a point (point match) or a circular area (circle match) can be targeted at each fundamental frequency, while harmonic sectors can be targeted at the harmonic frequencies (see Figure 34). The area of each harmonic sector is defined by two intersecting lines, the Smith chart edge, and the sequence in which the two Smith chart edge intersects are specified. The intersect of the two lines (local origin) must be inside the Smith chart and rotation from the first to the second point is assumed to be clockwise. (*A* to *B* in Figure 34. The complementary area will be targeted if point B is specified as the first point.)

Harmonic traps (attenuation poles; [12]) can be introduced in the design by adding fixed-element sections to the circuit before the matching network is synthesized (Specifications | Terminations | Fixed Elements command in the Matching module). Information on potential second-harmonic and third-harmonic traps is provided during the load-pull phase (CIL wizard). The viability of each of these traps is also considered when this is done. A harmonic trap will not be useful if it loads the fundamental frequencies significantly.

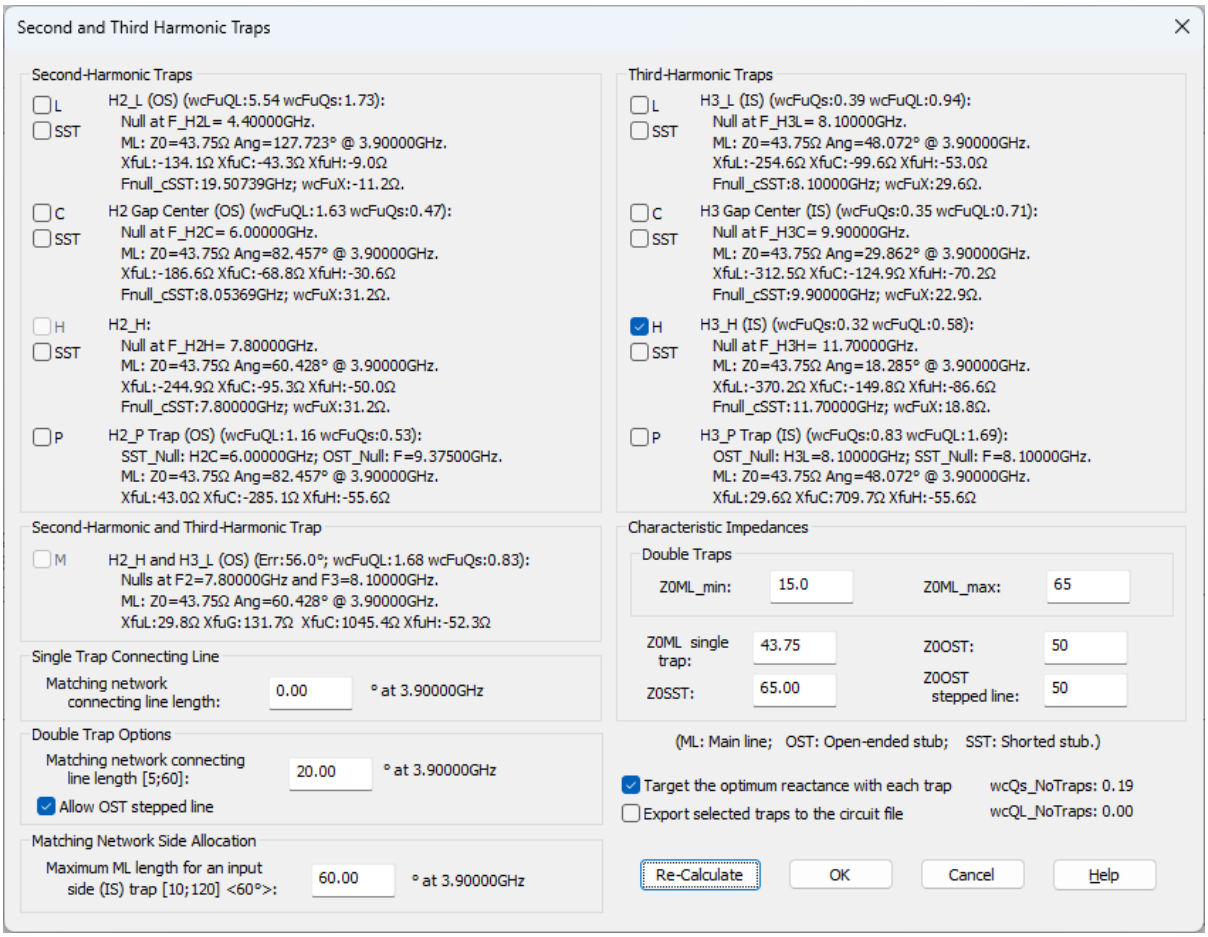

Figure 35. The list of potential traps provided by the CIL wizard. The characteristic impedances used can be edited and a few options are also provided. Use the Re-Calculate command to update the table after changing the specifications.

When possible, a trap should be used with a series-connected transmission line to transform the short or open associated with the trap to the intrinsic load impedance required at the trap frequency [13]. If the required line is electrically short and the fundamental-frequency loading is not severe, the trap could be added to the circuit before the matching network is synthesized. Information on the series-connected transmission lines required are also listed in the table created (see Figure 35).

Up to two traps can be selected from the trap table. If two traps are selected, one must be on the input side (IS) of the matching network (short main-line section), while the other must be on the output side (OS; longer main-line section). The side is decided by the specification for the Maximum Main-line Length for an Input Side Trap specification (see Figure 35). Note the option to export the selected traps directly to the circuit file. If this option is not selected, the next step will be to synthesize the load matching network.

An open-ended stub (90° long at the trap frequency) or a shorted stub (180° long at the trap frequency) can be used to provide the transmission null required at a trap frequency. The default is to use an open-ended stub. Click the SST option provided in the table to switch to using a shorted stub.

If *Z0OST* Stepped Line in the table is specified to be different from *Z0OST*, the open-ended stubs will be replaced with shunt branches consisting of a connecting line terminated in an open-ended stub. The electrical lengths of the two lines will be the same and will be set to provide resonance at the trap frequency.

The input side (IS) third-harmonic trap (H) selected in Figure 35, will provide a transmission null at 11.7GHz. The transmission line required to transform the harmonic short to the intrinsic impedance required for Class-B operation is relatively short (18.285° at 3.9GHz) and the fundamental loading is higher than 86.6Ω. The fundamental impedances on the input side of the matching network to be designed vary from around 28 Ω to around 16 Ω. The fundamental-frequency loading by this trap will, therefore, be light. The worst-case *Q*-factors (*X*/*R*) of the source terminations (*wcQs*) and load terminations (*wcQL*) of the matching network will be degraded from 0.19 to 0.32, and 0.0 to 0.58, respectively. The loading effect from a *Q* perspective is, therefore, also small.

The synthesis algorithm for non-commensurate networks was enhanced to provide for traps in the synthesized matching networks. (In commensurate networks the electrical line lengths are controlled, and the stub lengths can, therefore, be set for trapping.) Shunt capacitive branches (OST branches) or shunt inductive branches (SST branches) in a matching network can now control the fundamental-frequency performance and can also provide resonance at the transmission-null frequency specified.

Different resonant frequencies can be specified in the ADW for the capacitive branches and the inductive branches (See Figure 36). The trap frequency for inductive branches must be lower than the trap frequency for the capacitive branches. If the resonance frequency is specified to be higher than five times the highest passband frequency, only the fundamental frequency performance will be controlled.

When a shunt capacitive branch is designed, a connecting line terminated in an open-ended stub is used to provide the dual control [12, 13]. The default characteristic impedance and length of the connecting line can be modified by the user, while the electrical length and the characteristic impedance of the open-ended stub are the variables. When it is not possible to provide dual control, only the fundamental-frequency performance will be controlled.

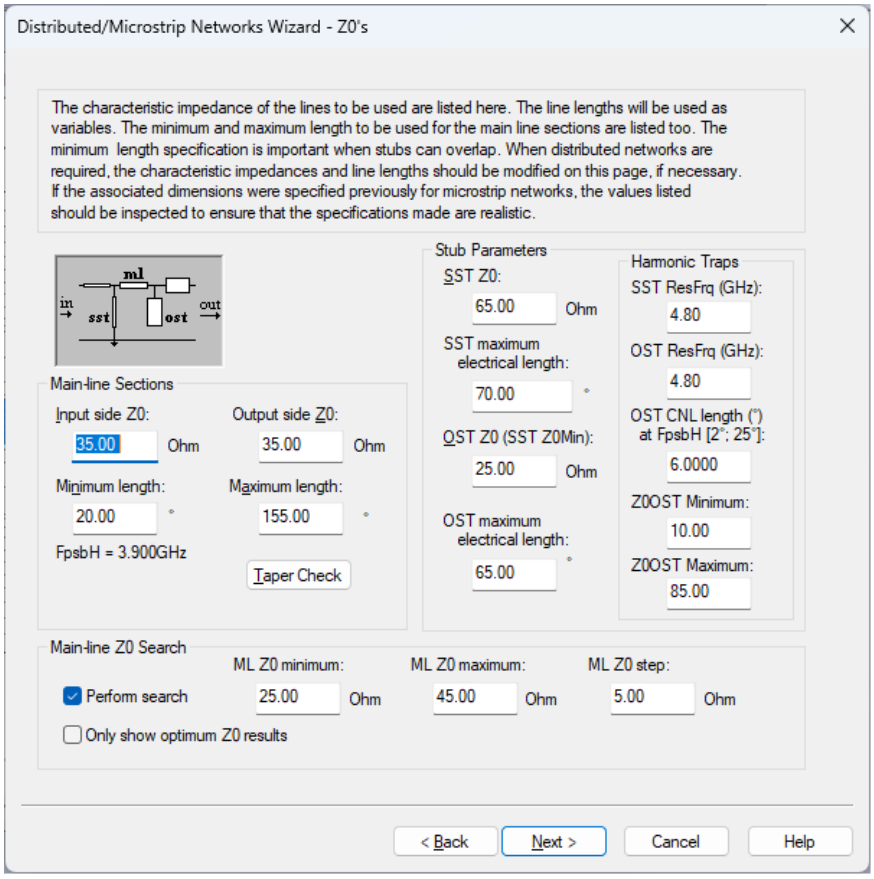

Figure 36. The specifications to be made for the distributed components in a non-commensurate distributed matching network.

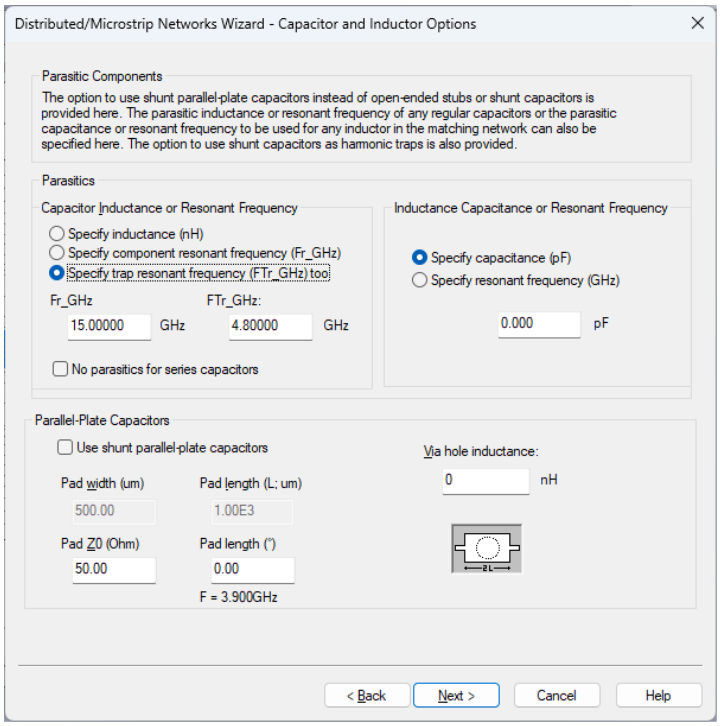

Figure 37. The options provided for the lumped elements in a mixed lumped/distributed matching network.

Each shorted-stub branch can be complemented with an open-ended stub branch to provide dual control. The length of the shorted stub is set to provide the transmission null required (similar to the

commensurate case). The complementary open-ended stub branch is used to modify the fundamental-frequency impedance of the shorted stub to the impedance required.

It is usually advisable to set the characteristic impedances for the shorted stubs as high as possible. *OST Z0* should be on the low side but is limited by the associated main-line discontinuity effects. *Z0OST* Minimum and *Z0OST* Maximum in Figure 36 apply to the open-ended stub termination of a shunt capacitive branch.

The functionality described above is also provided when shunt-connected capacitors or series-connected inductors are used. Parasitic inductance is added to a shunt-connected capacitor for this purpose, while parasitic capacitance is added to a series-connected inductor (See Figure 37). Short-circuit transmission nulls are associated with the shunt capacitors, while open-circuit nulls are associated with the series-connected inductors. When the transmission-null option is not selected, the parasitics specified for the lumped components can be fixed or can be calculated from the resonant frequency specified for the component type (capacitor or inductor).

A matching network with traps was shown in Figure 19 above. The trap specifications used are shown in Figure 38 (Passband: 1.0 – 3.9GHz). Note the 42Ω 10° line on the input side of the matching network (Figure 19). This is a fixed component added to rotate the intrinsic impedance obtained with the matching network clockwise.

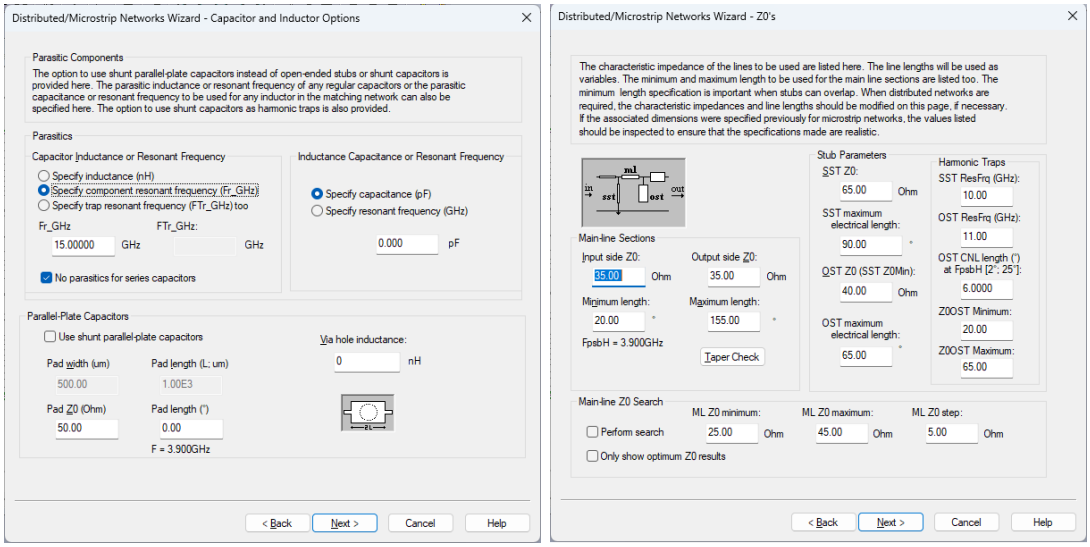

Figure 38. The traps specifications for the network shown in Figure 19.

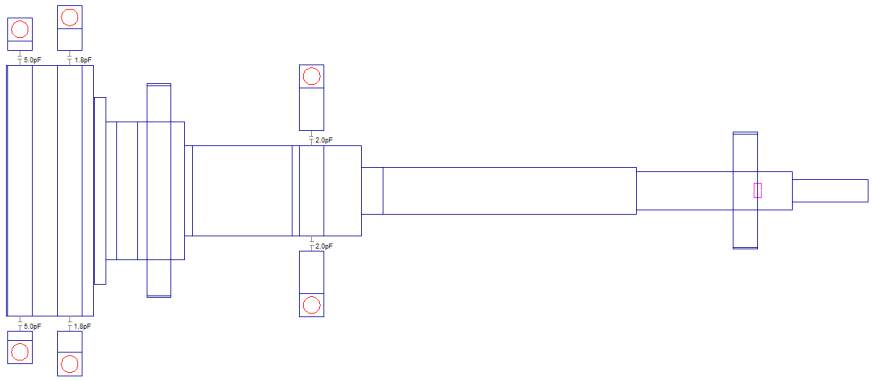

Figure 39. The artwork of an ADW matching network designed by using *S*-parameter based models for the microstrip junctions.

An example of a power matching network designed without using the harmonic trap options is shown in Figure 39. *S*-parameter based models were used for the microstrip junctions in the final version of the circuit. The parasitic inductance for each capacitor was set to 0.3nH.

Basic distributed matching networks can now also be synthesized in the ADW to provide a conjugate match and a specified transmission phase shift at a chosen frequency in the passband [10]. To minimize to reflection over the passband, a two-dimensional search on the transmission phase-shift and the main design parameter associated with each of the network types can be done. A specific phase-shift can also be targeted in the search. Circular fundamental-frequency matching areas are use as targets in the passband, while Smith chart sectors are targeted at the second and third harmonic frequencies.

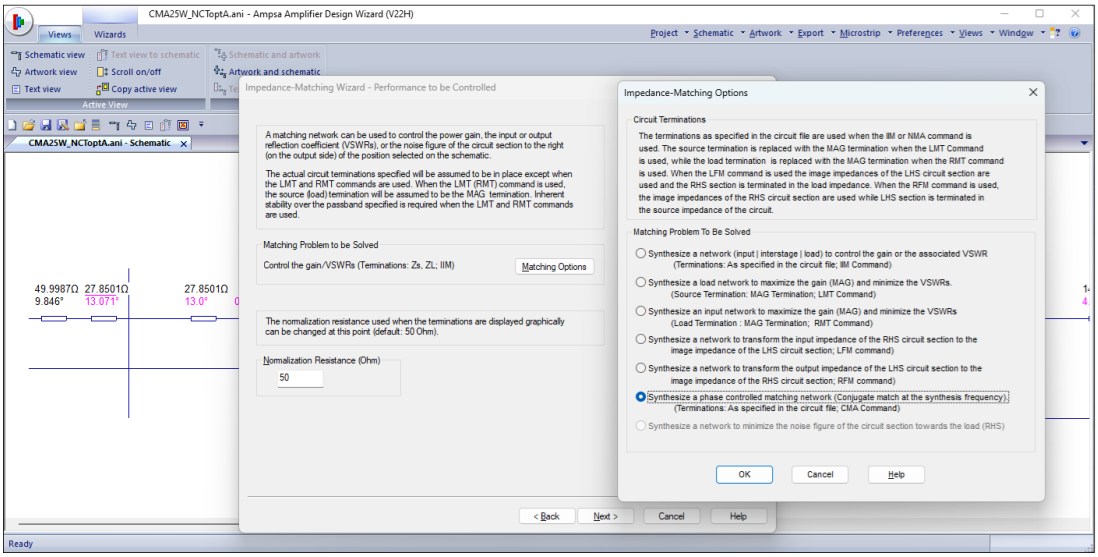

Figure 40. The CMA option provided by the IIM wizard is used to design phase-controlled matching networks in the ADW.

Use the CMA matching option provided by the IIM wizard to synthesize phase-controlled matching networks. The insertion point for the matching network must be selected before launching the IIM wizard. The phase-controlled matching (PCMA) options provided are shown in Figure 41.

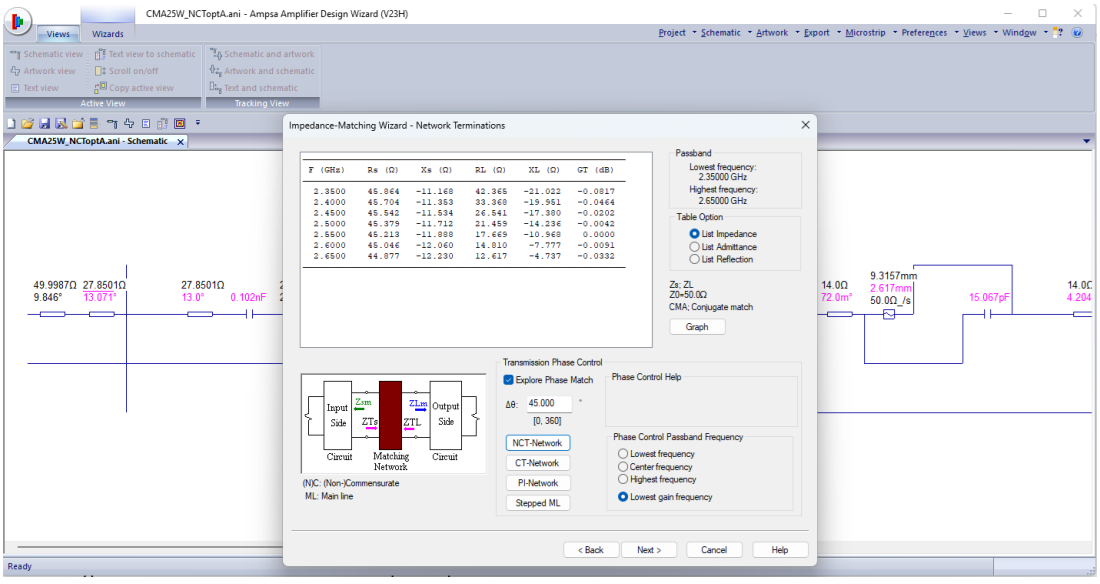

Figure 41. The phase-controlled matching network options provided in the ADW.

The network types currently allowed when the transmission phase-shift is controlled are non-commensurate or commensurate T-networks (see Figures 42 − 44), PI-networks and stepped lines. The shunt section(s) of the T- or PI-networks can be distributed or lumped (with pads for the lumped components), and may consist of a single element, identical parallel elements, or resonating sections. When resonating sections are used, the two-dimensional search becomes three-dimensional. The line length or the characteristic impedance of a shunt line can be controlled by the user. The length should usually be controlled when harmonic sectors are targeted.

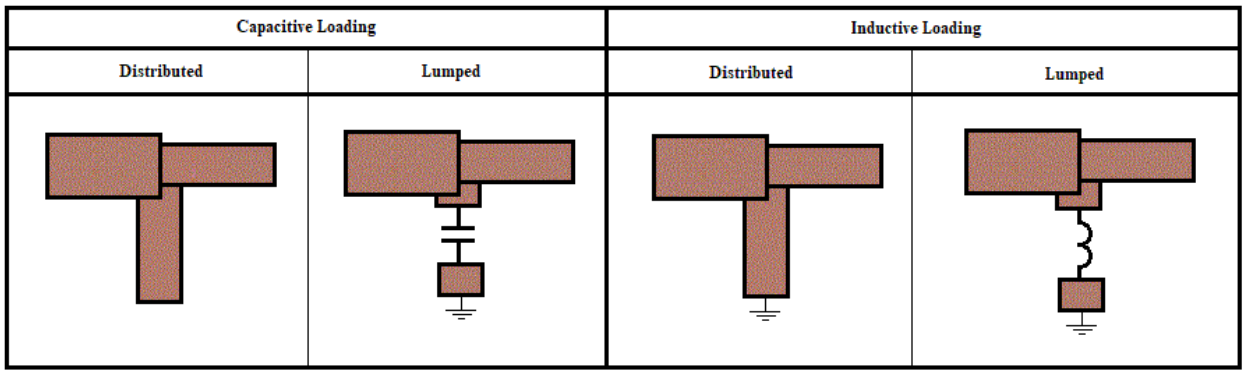

Figure 42. The main line of a commensurate T-network can be loaded with an open-ended stub, a shorted stub, or a lumped equivalent with pads.

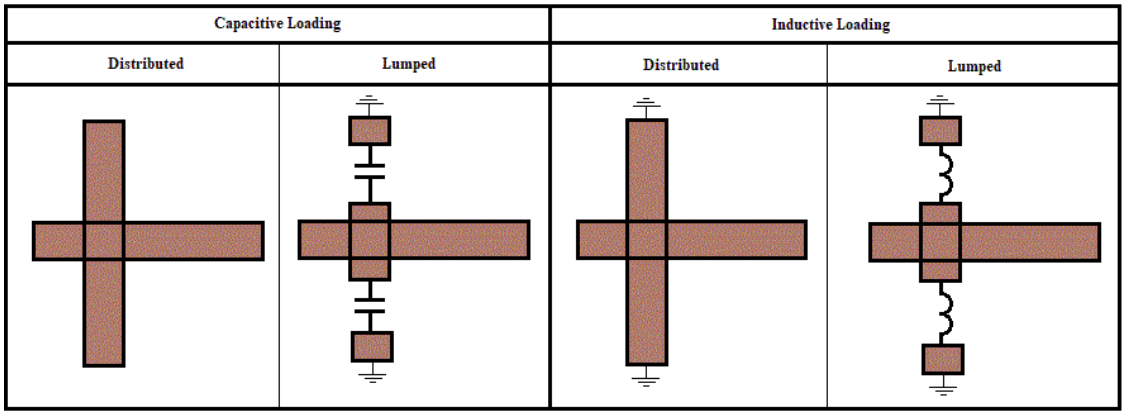

Figure 43. The commensurate T-network topologies associated with the Parallel Shunt Elements option are shown here.

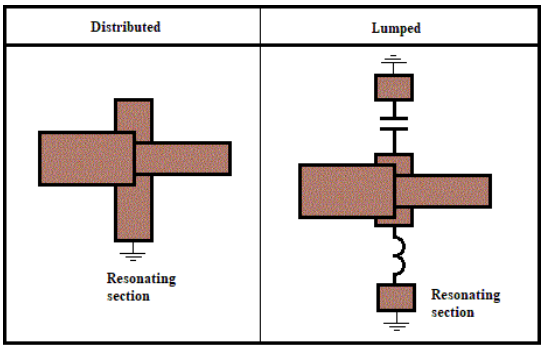

Figure 44. The non-commensurate T-network topologies associated with the resonating sections option.

The parameters to be specified and the options provided when a systematic search for the best PCMA network is done are shown in Figure 45. It may be necessary to increase the maximum value for the input or output VSWR to get solutions to the problem to be solved. Non-commensurate T-networks are targeted in Figure 45. The main design parameter is the characteristic impedance of the two main-line sections. Note that the range for the characteristic impedance can be constrained.

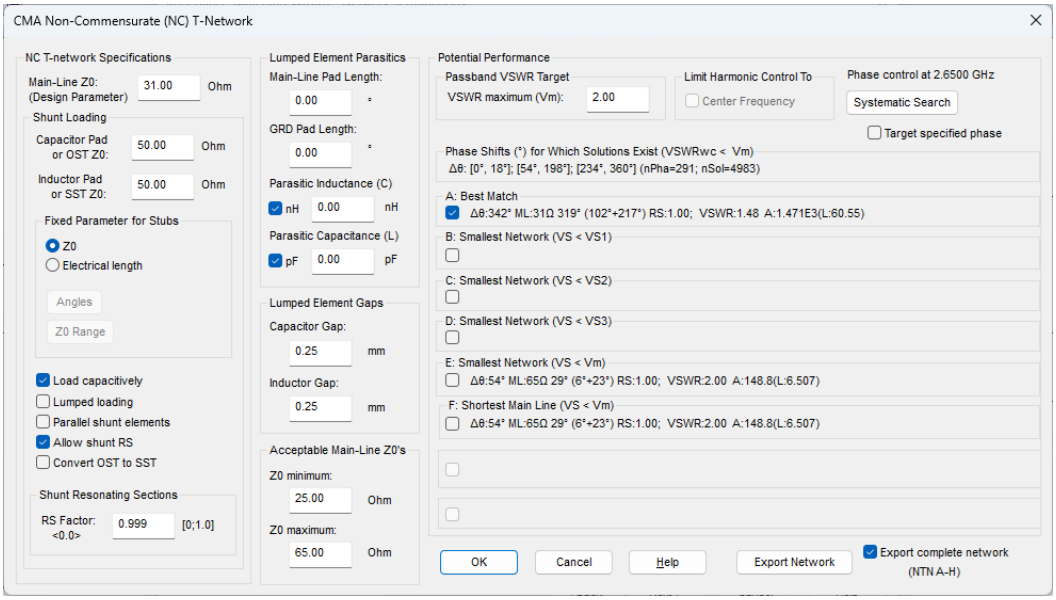

Figure 45. The parameters to be specified and the options provided when a systematic search is done for the best phase-controlled solution to a matching problem in the ADW.

Circular areas at the fundamental frequencies and sectors at the second and third harmonic frequencies can also be targeted with PCMA networks. An example of such a search is provided in Figure 46. Note the F: 6 3 0 string in this figure (Solution G). This indicates that the fundamental frequency targets were met at six frequencies (reflection coefficient inside a circle targeted). The second harmonic targets were met at three frequencies (reflection coefficient inside a sector targeted) and the third harmonic is off target. Also note the option to limit the harmonic control to the centre frequency in each harmonic band.

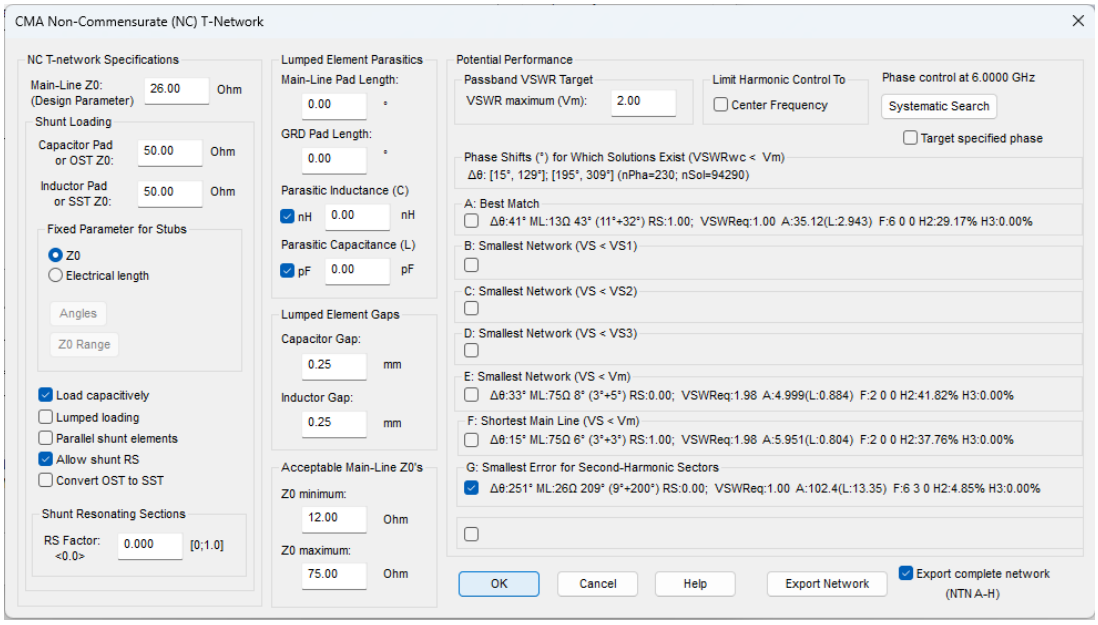

Figure 46. Fundamental-frequency circles and harmonic sectors were targeted in the search shown here.

The input reflection coefficients of a commensurate T-network are compared in Figure 47 with the fundamental-frequency targets (F) and the harmonic targets (H2; H3). The original second harmonic and third-harmonic markers are used in the comparison instead of the harmonic sectors fitted to these markers. (The fitting is automatic in the ADW.)

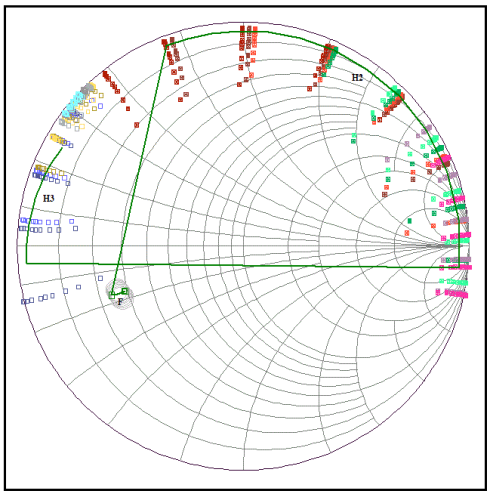

Figure 47. Comparison of the input reflection coefficients presented by a commensurate T-network with the fundamental-frequency targets (F) and the harmonic targets (H2; H3).

The reflection coefficients of a passive network can only rotate clockwise. It is, however, possible to obtain approximate anticlockwise behaviour with resonant loops in the reflection coefficient trace (see Figure 48). If the design parameters for the mode are set for anticlockwise rotation of the fundamental-frequency reflection coefficients with increasing frequency, clockwise rotation of the harmonic targets will not be an issue. To get the output power close to the expected level, the correct harmonic roll-off will also be required.

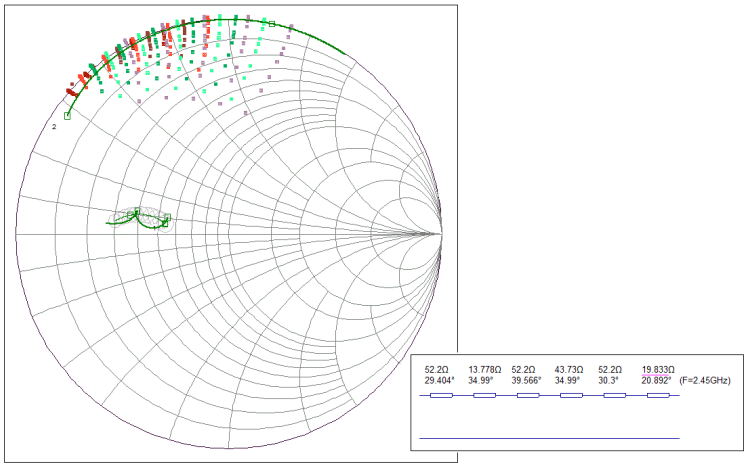

Figure 48. The input reflection coefficients of a matching network for fundamental-frequency targets that rotate anticlockwise with increasing frequency.

An alternative to anticlockwise fundamental-frequency targets is to set all the fundamental-frequency intrinsic targets to be inductive, with the second-harmonic targets capacitive. Depending on the bandwidth, this could yield some continuous-mode behaviour at all the frequencies of interest. The design could be done for full cancellation at the centre frequency.

The continuous inverse Class-F mode example in [12] is a good example of the first approach. It targeted anticlockwise inductive reflection coefficients in the passband (Design parameter: [0,1] initially and around [0, 0.5] for the network designed) and clockwise capacitive second-harmonic reflection coefficients. The third-harmonic targets were also capacitive and were bundled in a narrow range. The fundamental frequencies (1.4 to 2.5 GHz) did not overlap with the second harmonics in this example. A second-harmonic trap at 2.8GHz was used to obtain the performance required.

The matching network designed in [12] is shown in Figure 49, with the input reflection coefficients calculated in the ADW and Sonnet Software's EM (thick metal; free space cover; third harmonic box resonances were flagged with full or partial suppression because of the free space cover). *S*-parameter based junction models were used in the ADW simulation. (The required *S*-parameters were generated in Sonnet.) The intrinsic reflection coefficients associated with the matching network as calculated in the ADW are shown in Figure 50. While the general trend correlates reasonably well with [12], some tuning is required to get a better fit.

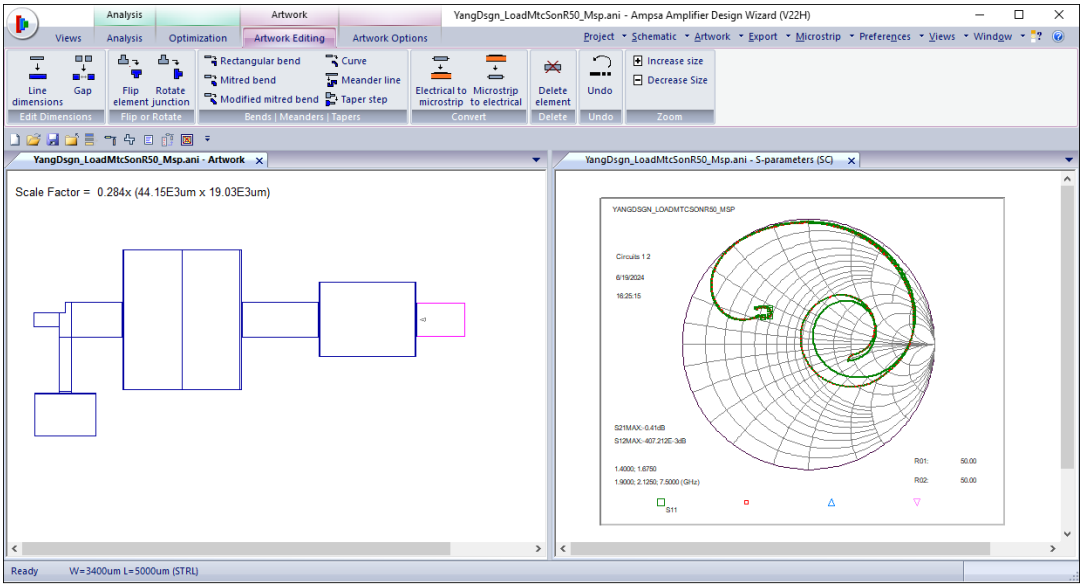

Figure 49. The matching network designed in [12] to obtain continuous inverse class-F behaviour as analyzed in the ADW with *S*-parameter based discontinuity models. The input reflection coefficients of the matching network are compared with the input reflection coefficients obtained with Sonnet Software's EM.

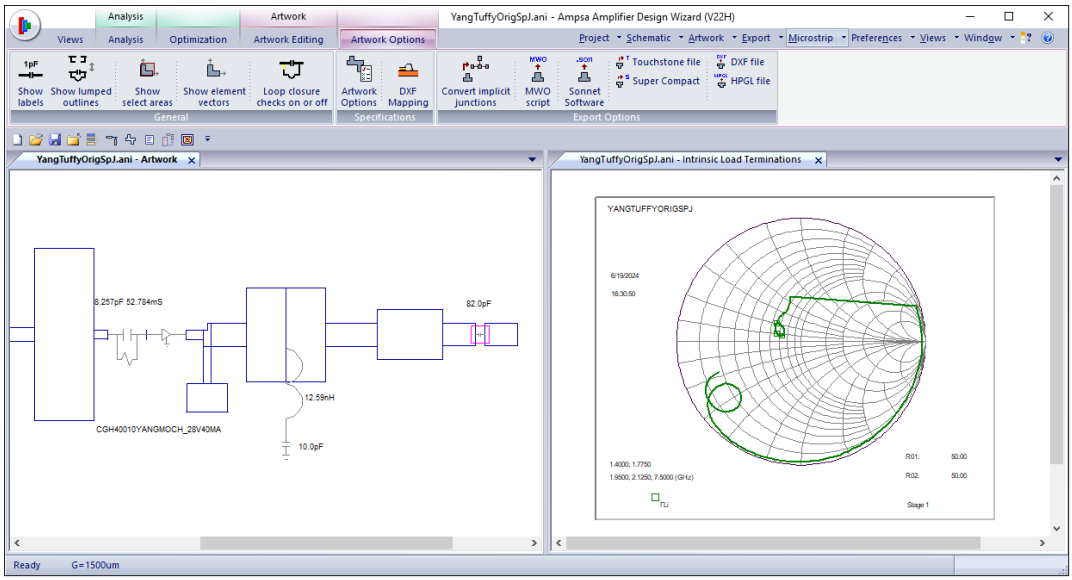

Figure 50. The intrinsic reflection coefficients for the design presented in [12] as calculated in the ADW.

An example of a single-stage wideband 10W amplifier designed with Version 22 of the ADW is provided in Figure 51. The Macom CGH40010F was used in this example. Harmonic traps were used to get the wideband performance. The intrinsic load reflection coefficients presented to the transistor and the dynamic load lines are also shown in Figure 51. The performance is essentially Class-B (with reduced second-harmonic content) over this very wide passband.

A new load network was synthesized for this amplifier by targeting the required intrinsic harmonic terminations directly. The network selected is shown in Figure 52 with the associated amplifier performance. This network is much simpler, and no optimisation was required to get the performance shown. The performance of the ADW schematic in Microwave Office™ is shown in Figure 53. The performance calculated in the ADW is shown on the right with the same scaling. Note that the frequency ranges are not the same.

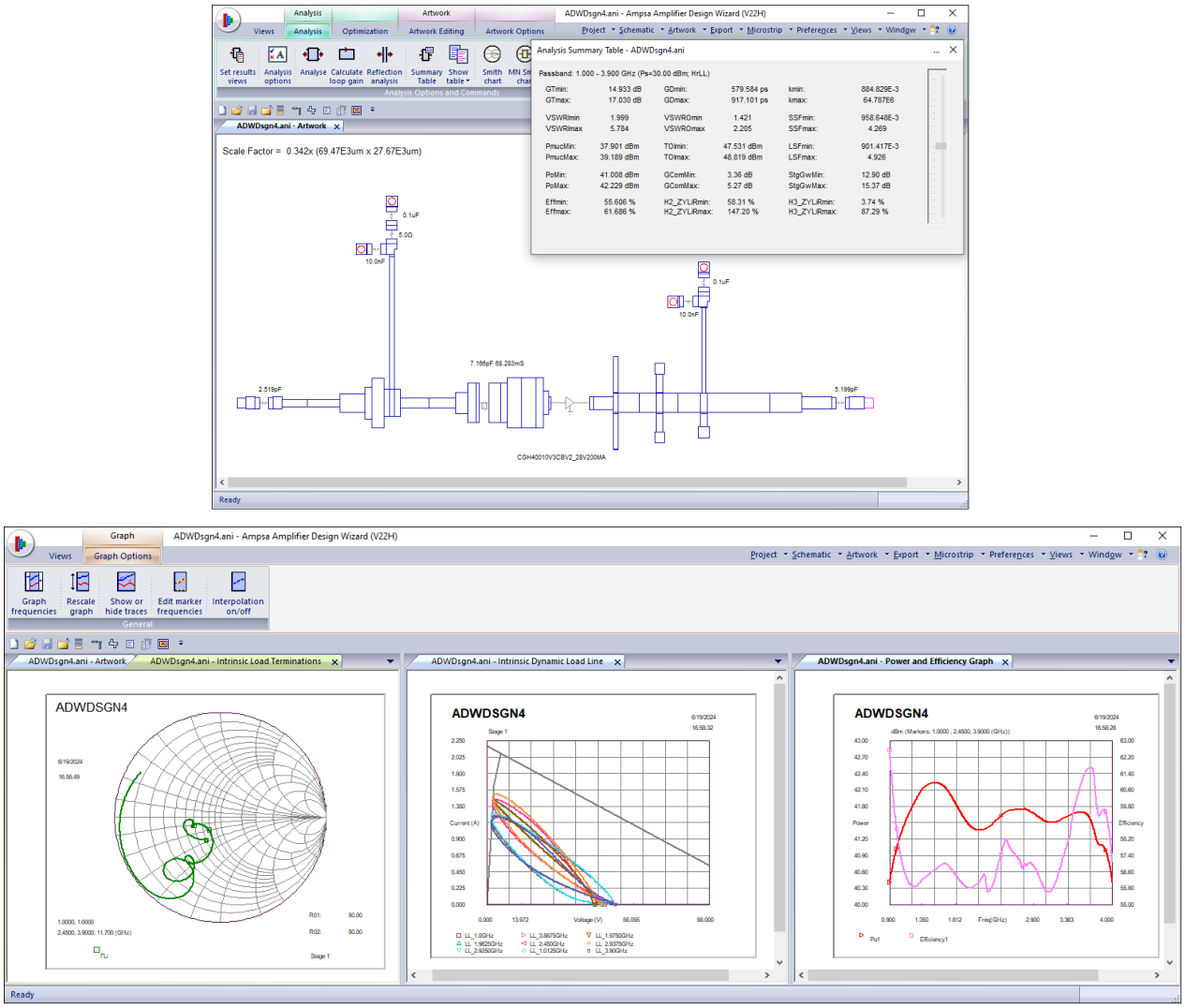

Figure 51. The ADW performance of a wideband 10W amplifier designed with harmonic traps. The passband is 1.0 – 3.9 GHz. This amplifier was designed with Version 22 of the ADW.

The design can be fined-tuned with harmonic-balance, EM-simulations and accurate models for the lumped components in Microwave Office™ or ADS™.

It is advisable to export the ADW artwork, as well as the electrical network (ADW schematic when using MWO or the *S*-parameters associated with each matching network when using ADS). The subcircuits in the electrical network (MWO) or the *S*-parameters (ADS or MWO) can be used as targets if adjustments to the artwork are required because of the differences in the microstrip models used and/or coupling between components. If the ADW design is first refined by upgrading the implicit microstrip models used to *S*-parameter based junctions, the correlation in the performance will be tighter.

Note that (at least) the second and third harmonics should be included in the *S*-parameters exported.

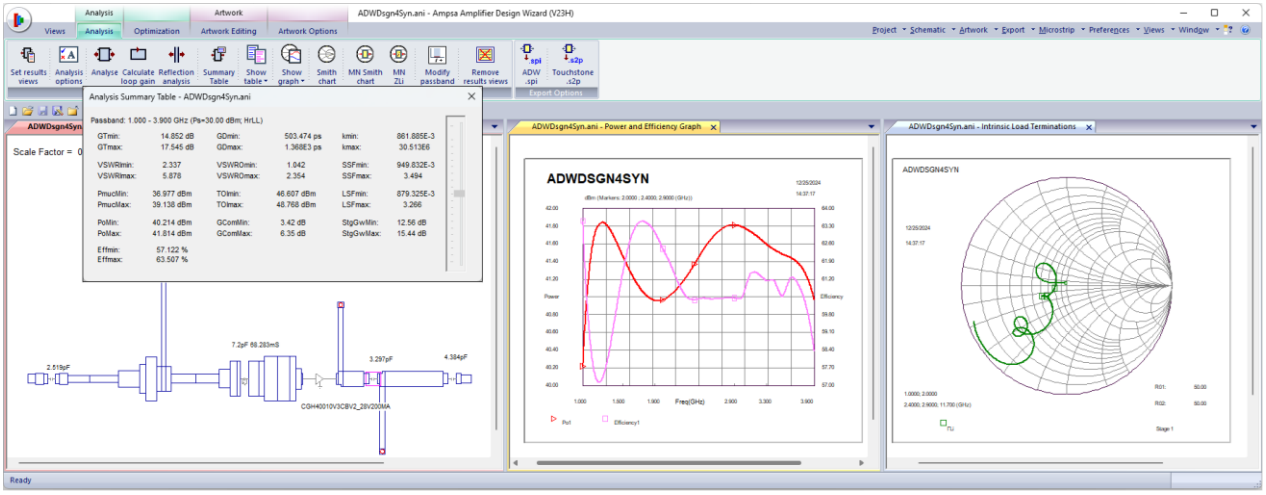

Figure 52. A new load network was synthesized for the amplifier shown in Figure 51 by using the new features provided in Version 23 of the ADW. This network is much simpler, and no optimisation was required.

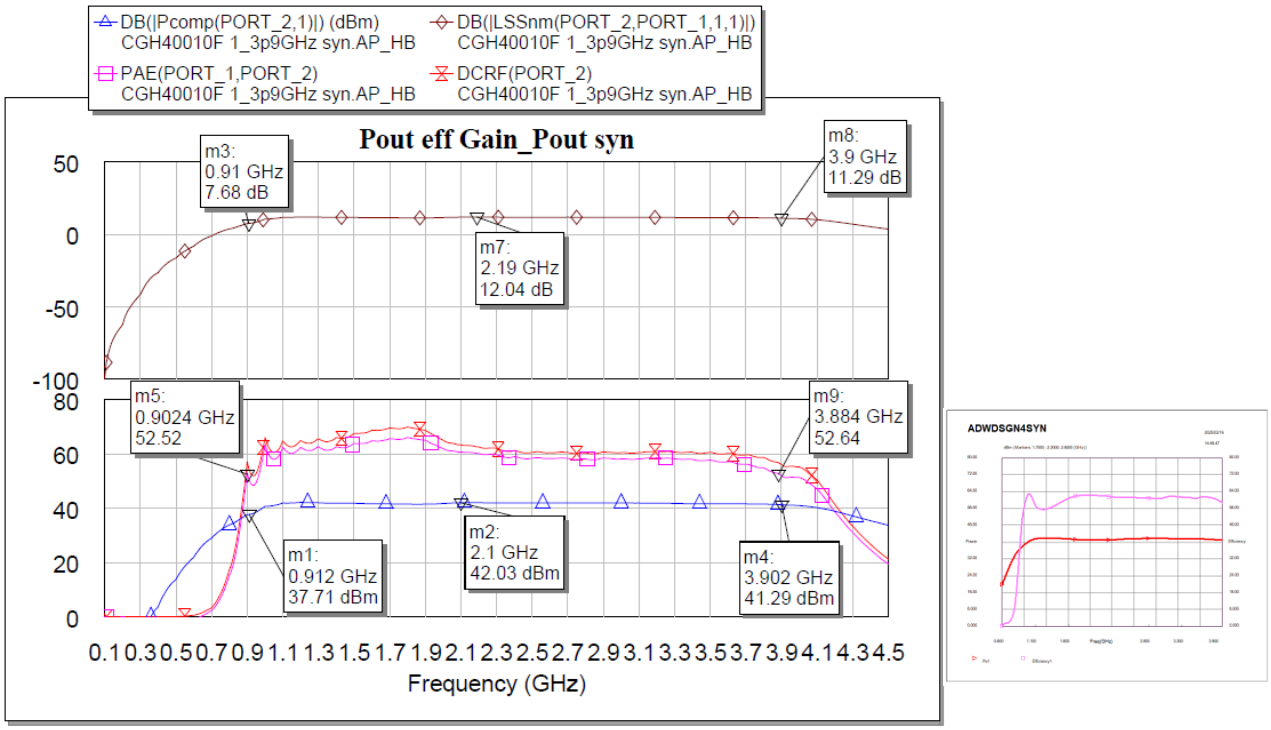

Figure 53. The electrical performance of the ADW amplifier in Figure 52 as analysed in the Microwave Office™. The red trace in the MWO plot is the drain efficiency and the magenta trace is the power-added efficiency.

Fitting an accurate model to a strong microstrip discontinuity over a very wide band can be challenging. For this reason, refining an ADW circuit by using *S*-parameter based junction models is good practice. The ADW design should be re-optimized after introducing the *S*-parameter based junctions, if necessary.

The implicit junctions of a complete ADW circuit can be converted to have *S*-parameter based junctions. The menu command used for the automatic conversion is shown in Figure 54. (Only the load network was converted in this figure.) The artwork of the ADW circuits created for the junctions must be exported for EM simulation. The length of the reference lines attached to the junctions must be specified when the implicit junctions are converted (see Figure 54). The resolution to be used in the artwork must also be specified. The resolution will impact the run times in the EM simulator used.

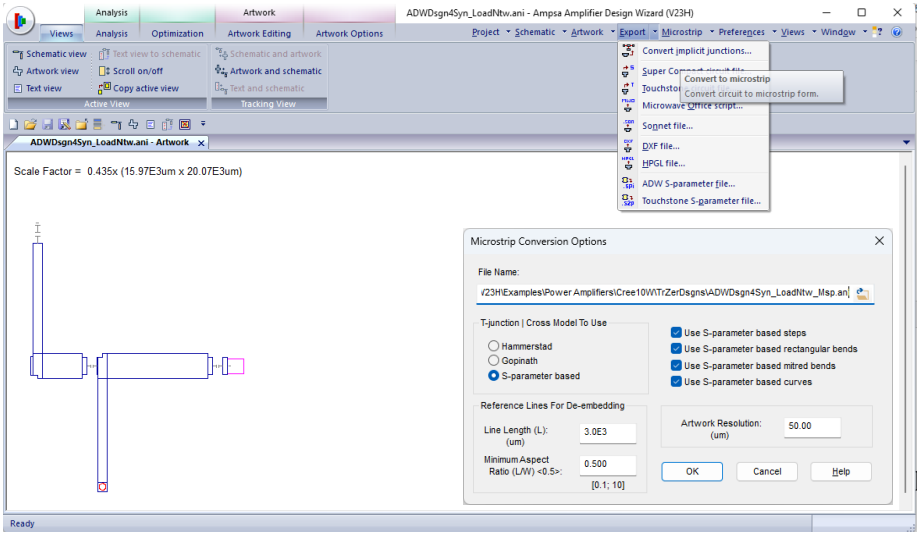

Figure 54. The command used to automatically convert the implicit microstrip junctions in the ADW artwork to explicit junctions. Note that the artwork resolution was reduced to 50 µm to speed up the EM simulations for the junctions to be exported.

Two T-junctions and two step junctions were converted in the load network. The changes in the s_{11} of the load network are shown in Figure 55 on a Smith chart. The changes are relatively small, and the amplifier performance changed only slightly with these changes. The effect on the input network is mild up to the highest second harmonic frequency. Sixteen step junctions and two T-junctions were converted in this network. The EM simulations were done with Sonnet.

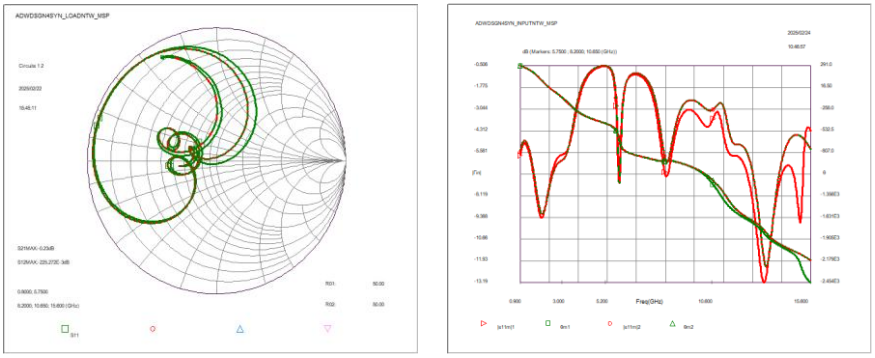

Figure 55. s_{11} of the load network and the input network in Figure 52 (implicit junctions) are compared here to the s_{11} after introducing *S*-parameter based junctions into the networks.

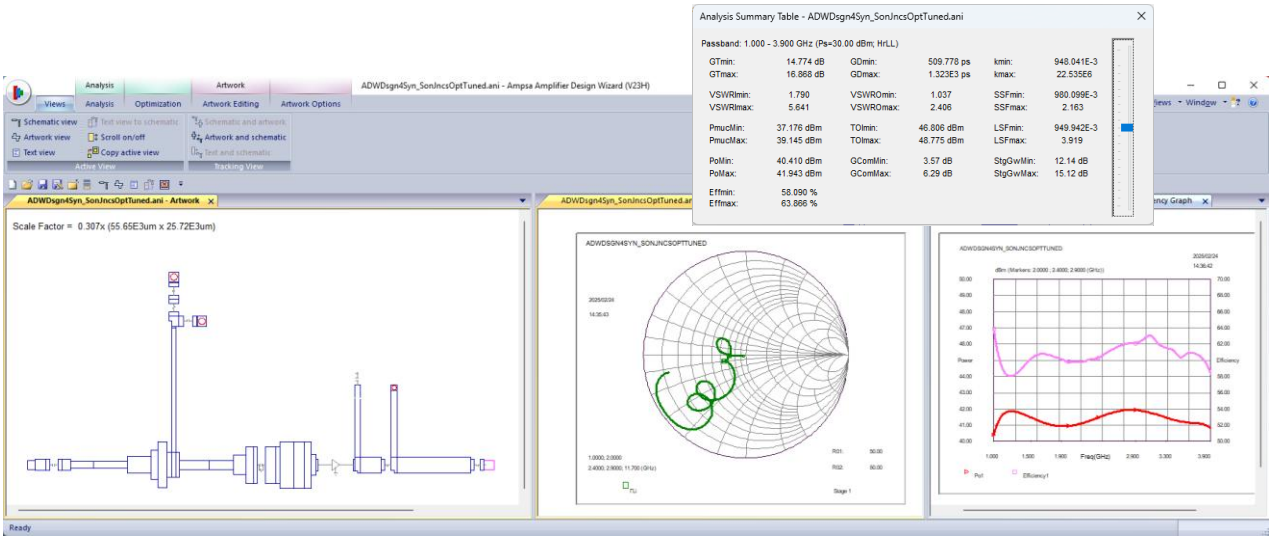

Figure 56. The performance of the amplifier after optimisation of the input network and tuning of the load network.

With the *S*-parameter based junctions in place, the input matching network was optimised to improve the gain, the input and the output VSWRs and the stability. The load network was then tuned to improve the efficiency without moving the intrinsic harmonic terminations away from Class-B operation and without lowering the power level. The amplifier is shown in Figure 56 with the ADW performance obtained.

Note from the summary table shown in Figure 51 that the amplifier is conditionally stable at all the frequencies considered (0.1 – 20 GHz; *SSF* > 0.95 and *LSF* > 0.90), where *SSF* is the source stability factor and *LSF* the load stability factor. *SSF* and the *LSF* are generalized versions of *mu-prime* and *mu* [16], respectively. Assuming arbitrary angles for the mismatch reflection coefficients, positive values for *SSF* and *LSF* indicate how much the actual source or load termination can change (expressed as complex-normalized reflection coefficients) before the circuit may become potentially unstable.

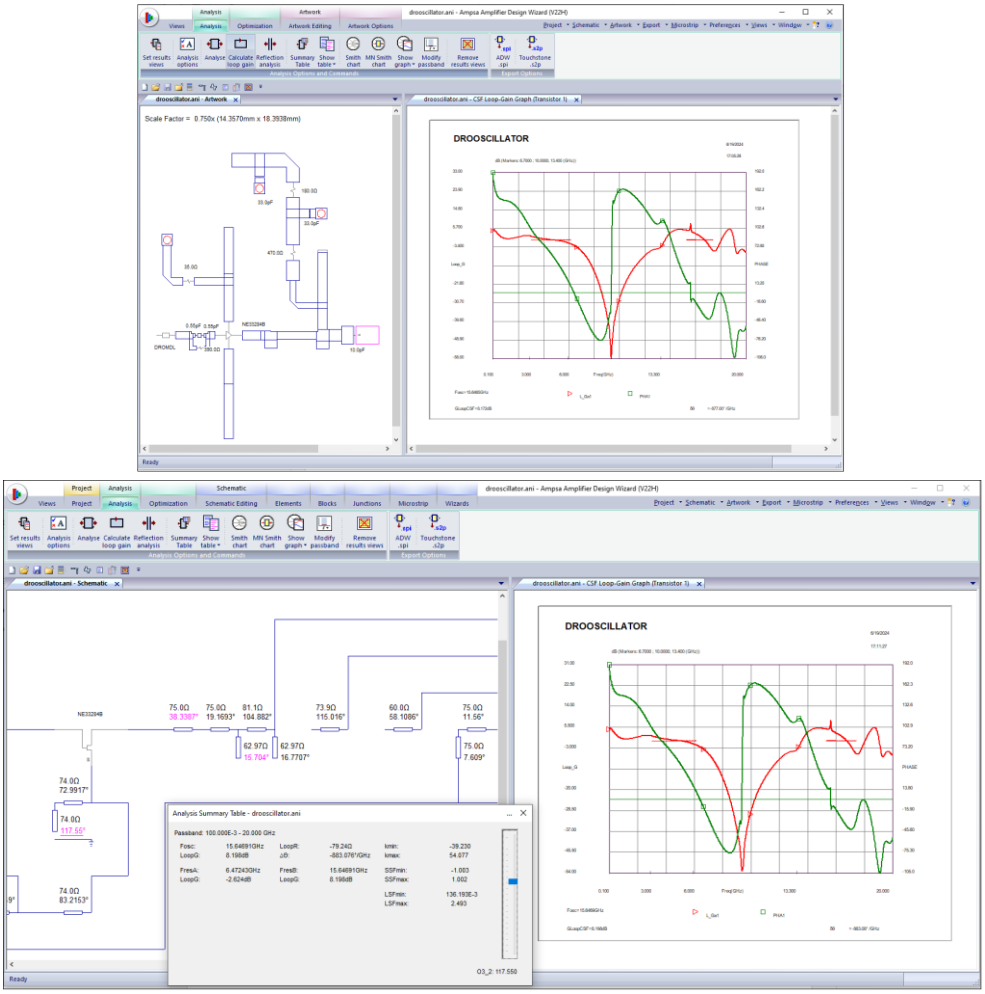

Figure 56. The loop gain of a DRO oscillator is displayed here. Note that the tuning feature is active when the summary table is opened on a variable marked for optimization.

SSF and *LSF* are black box stability factors. When feedback is applied to a transistor the loop gain provides additional insight into the stability of an amplifier or the behaviour of an oscillator. The loop gain for each transistor (with feedback) in an ADW circuit can be calculated by using the Loop Gain Analysis command provided. A Bode plot of the loop gain for a dielectric resonator oscillator is shown in Figure 56. The phase of the gain is zero at two frequencies, but the loop gain is less than zero (gain margin) at the first frequency. The capacitor in series with the dielectric puck is used to prevent oscillation at the first frequency. Note the high slope in the phase at the oscillation frequency. The horizontal red segments at the unity gain level are used to mark the frequencies with zero or negative resistance in the feedback loop.

Also note the summary table displayed in Figure 56. The frequencies at which the phase of the loop gain is zero are listed in the table with the associated loop gain values. Up to ten zero crossings can be listed. The tuning feature is also active when the loop gain is calculated. Insight into the behaviour of the oscillator can be gained by tuning the components.

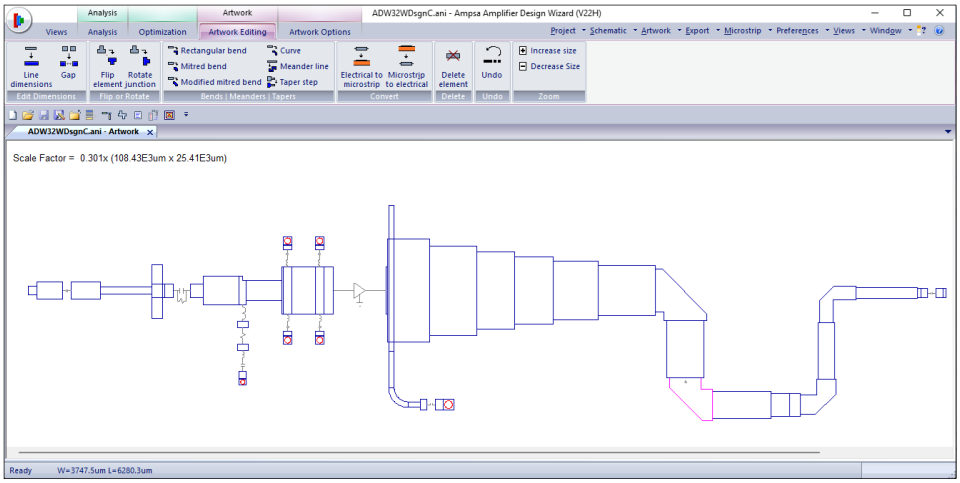

Figure 57. A 30W amplifier designed by using a geometric-mean stepped taper. The passband is 0.65 – 2.65 GHz.

A geometric-mean taper is used in the ADW amplifier shown in Figure 57. A 45 W Macom CGH40045F was used in this example to design a wideband 30 W amplifier (0.65 – 2.65 GHz). The power contours and maximum efficiency lines shown in Figure 6 were generated for this transistor. The performance as analysed in the ADW is shown in Figure 58.

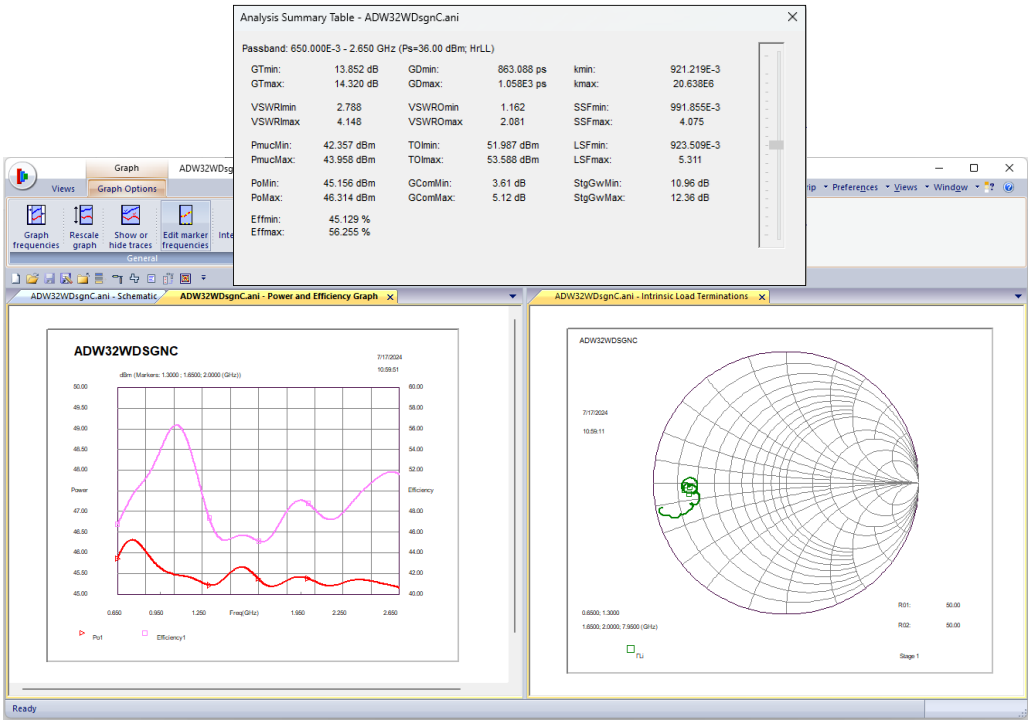

Figure 58. The power and efficiency of the amplifier in Figure 57 as analysed in the ADW. The intrinsic load reflection coefficients are shown on the right (0.65 – 7.95GHz).

The electrical performance of the ADW design as simulated in Microwave Office™ is shown in Figure 59. The output power and the efficiency calculated in the ADW were scaled similarly and are shown on right.

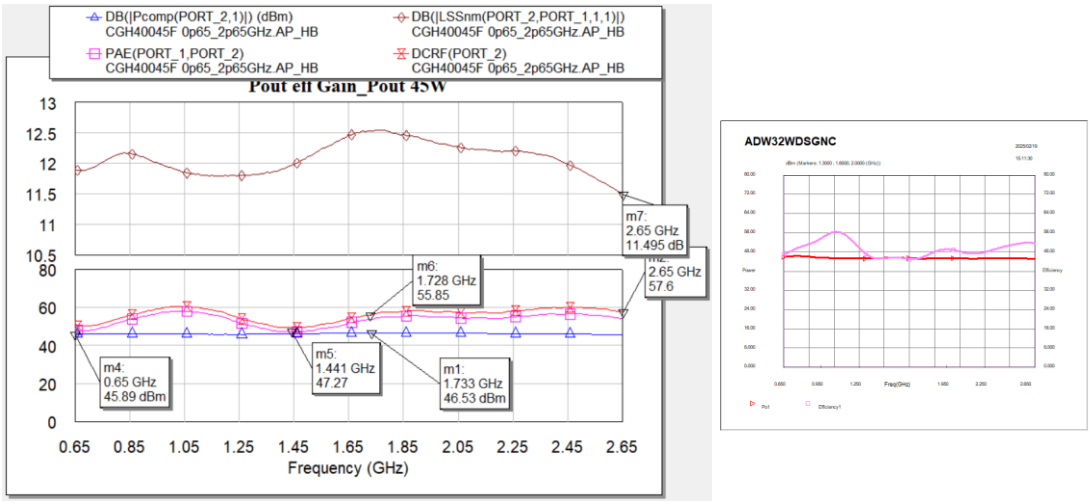

Figure 59. The electrical performance of the ADW amplifier in Figure 57 as analysed in the Microwave Office™.

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