Single-Ended Equivalents for Symmetrical Power Amplifier Combination Networks

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The Ampsa Amplifier Design and Matching Wizards were developed to primarily design single-ended amplifiers, but symmetry can be used to transform symmetrical transistor combining networks to single-ended equivalents. An example is provided in Figure 1. (Z_{HALF} and Z_{DBL} are ideal transformers.) The voltages in the symmetrical circuit and the single-ended equivalent are identical. The input and output currents of the transistor in the single-ended equivalent and the associated transistor in the symmetrical circuit are also the same.

If a driver amplifier is used, the power extracted from the single-stage equivalent, as well as the *dc* current required by it, must be multiplied by four when the efficiency is calculated in the example shown. (Use the Project | Options menu command to set the relevant scale factors.) This is required to keep the efficiency calculations in agreement.

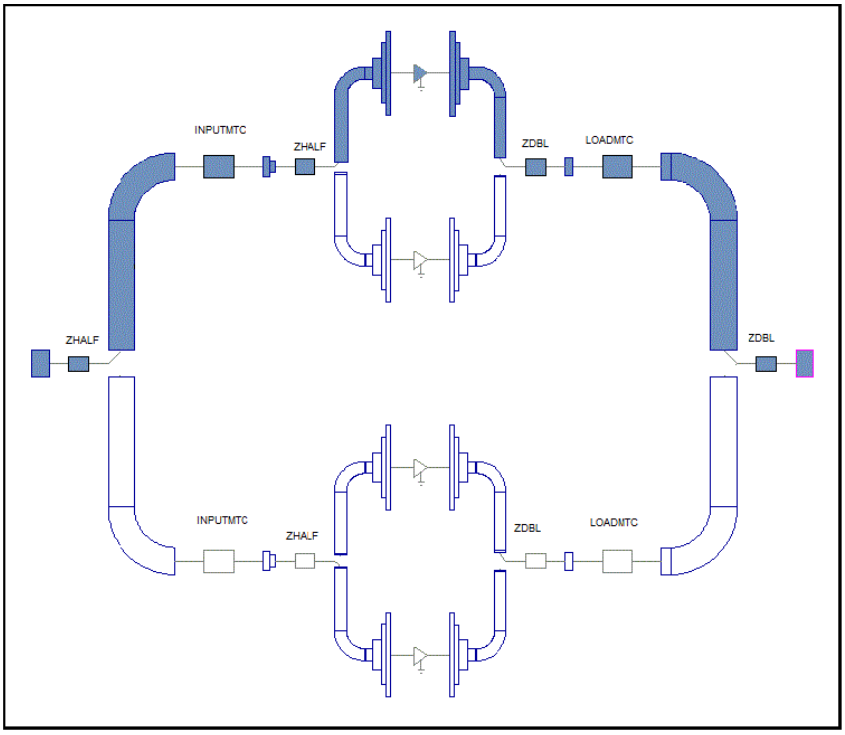

Figure 1. Illustration of the process to simplify the design of a power stage with symmetrical combining networks to designing a single-ended stage.

T-section models (three cascade networks joined at a common node) must be used for the microstrip T-junctions in the original circuit and the equivalent circuit. This is required to not disturb the impedance scaling and the open circuit conditions required.

Explicit or implicit junctions (steps, T-junctions, and crosses) can be used in the ADW/MW. The implicit junctions are defined by the lines forming the junctions and are detected and processed automatically. Implicit junctions are used when matching networks are synthesized in the ADW or the MW.

Explicit junctions are required at the symmetry points of the symmetrical combining network before the single-ended equivalent can be created. An ADW/MW schematic with implicit junctions can be transformed automatically to microstrip form (with explicit junctions) by using the Export | Convert Circuit to Microstrip Form menu command. The electrical lines in the schematic are then transformed to dispersive microstrip lines at the conversion frequency specified (Project | Substrates menu command), and the implicit steps, T-junctions and crosses are replaced with explicit junction commands. See Figure 2 for an example. (Note that the artwork of the circuit to be converted must be viewed when the conversion command is used.)

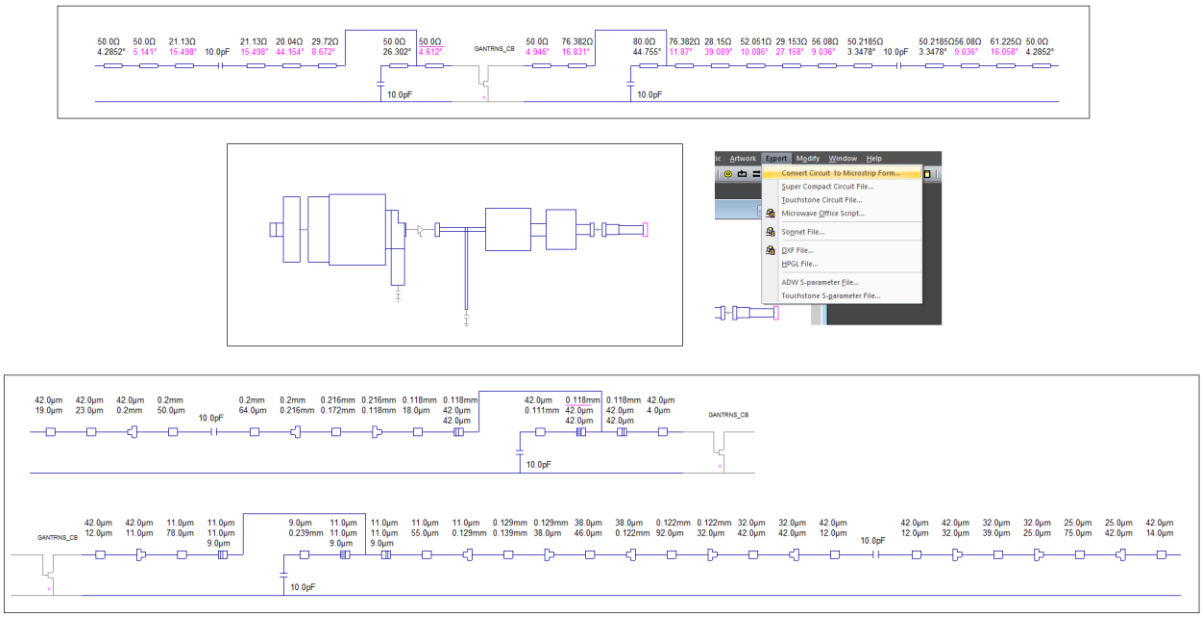

Figure 2. The electrical description for a single-stage amplifier was transformed to microstrip form in this example.

Basic Hammerstad models [1] are used for the implicit junctions (see Figure 3). Only changes in the reference planes are accounted for when implicit junctions are used. The transformer and shunt loading effects are ignored. (This is acceptable when the shunt arm of a T-junction is not electrically wide.) These effects are modelled when explicit Hammerstad T-junctions are used. The option to use an extended Gopinath model [2] instead of the Hammerstad model is also provided (see Figure 4).

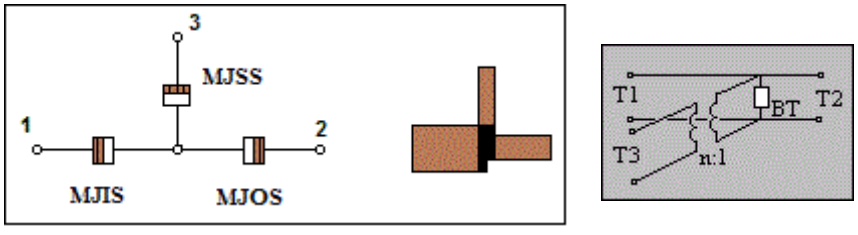

Figure 3. The Hammerstad model used for T-junctions in the ADW or MW (T-section model).

Three schematic elements are used to model a T-junction in the ADW/MW. The MJIS, MJOS and MJSS commands are associated with the Hammerstad model (refer to Figure 3), and the MLIS, MLOS and MLSS commands are associated with the extended Gopinath model. Four

elements are used to model a cross (Hammerstad: MJIS, MJOS, MJSS, MJSS; Gopinath: MLIS, MLOS, MLSS, MLSS).

The schematics for the ADW/MW junction elements are not symmetrical and the orientation of each element is important. The white space side of the schematic symbols associated with these elements must be on the common node side (see Figure 4).

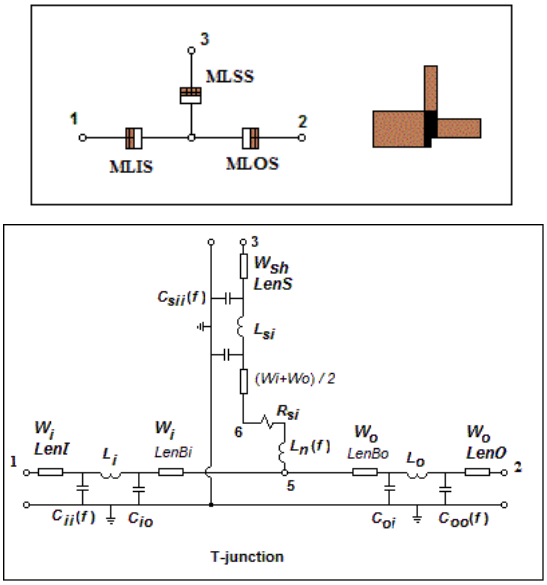

Figure 4. The extended Gopinath model used to model T-junctions in the ADW/MW.

When a T-junction is rotated to take the output from the shunt arm of the junction (see Figure 5), the MJSR command must be used in the shunt arm instead of the MJSS command. The schematic of the MSJR command is the reverse of that of the MJSS command (that is, the input and output nodes are reversed). The MJSS command is used when a junction is rotated to connect the shunt arm to a schematic element on the input side of the junction.

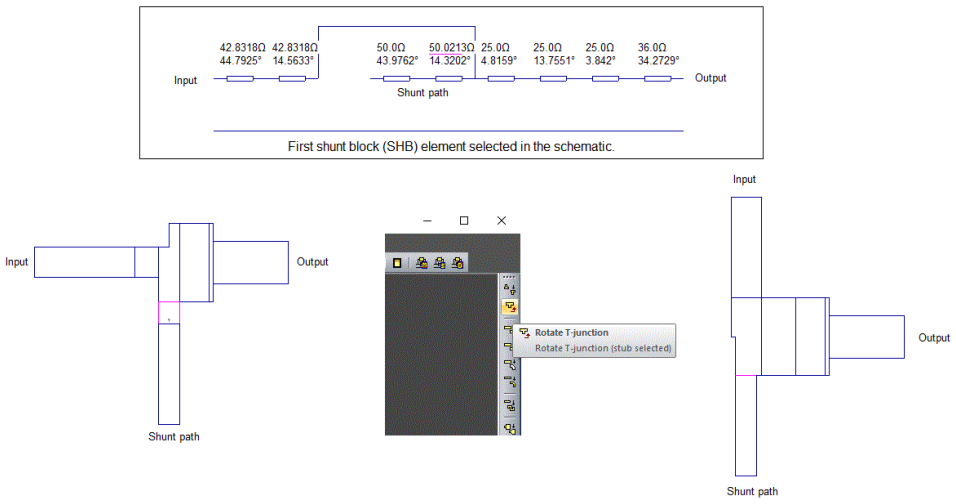

Figure 5. Illustration of changing the orientation of a T-junction in the ADW/MW. The selected element in the artwork is the first element in the associated shunt block (SHB).

The parameters associated with the T-junction or cross junction elements can be edited in an Artwork view (see Figures 6 and 7). The parameters provided for the Hammerstad model are used to scale the values in the standard Hammerstad model. The shunt loading (B_T) is usually placed in the MJSS element (shunt arm of the T-junction), but some loading is also allowed with the MJIS and MJOS elements. The offsets in the reference planes set the effective line lengths from the common node to the edges of the junction. Losses can also be specified for the junction elements.

The junction parameters can be optimized to fit the *S*-parameters obtained in an EM simulation of the junction. (The ADW/MW can generate a Sonnet Software® ".son" file for the artwork, and the schematic can also be exported to Microwave Office™ for simulation in Axiem™. DXF files can be exported for simulation in Momentum™.) Good results may be obtained by optimizing only the reference planes in the junctions. (Optimize more of the junction parameters if necessary.)

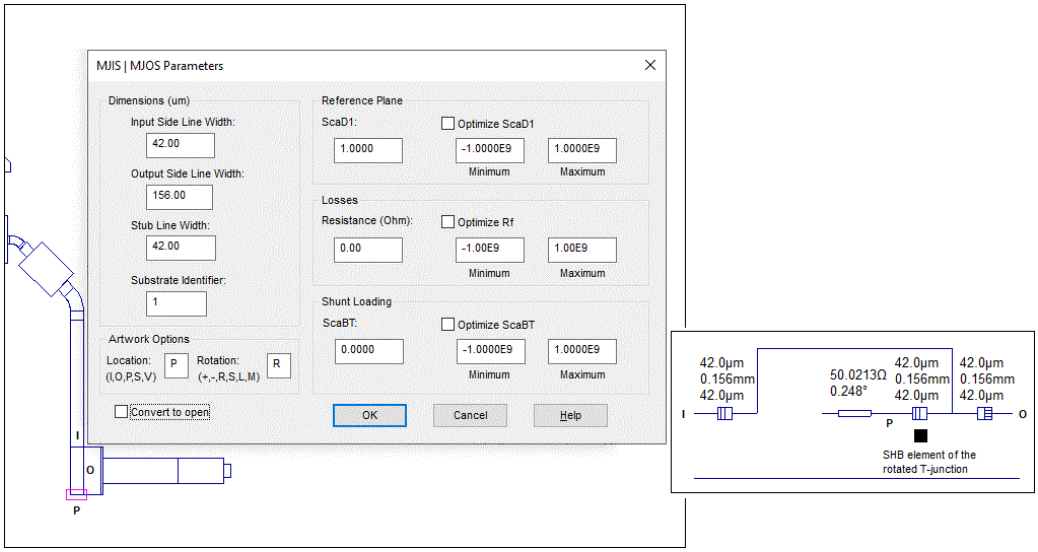

Figure 6. The option to open the path associated with a MJIS, MJOS, MLIS or MLOS command is provided when the command is edited in an Artwork view. The shunt block junction element is edited here.

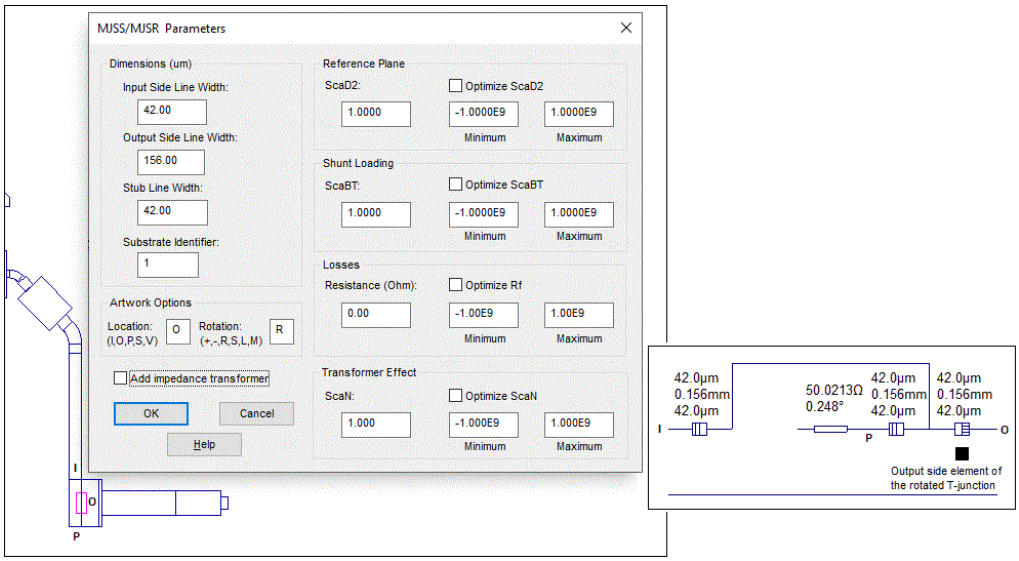

Figure 7. The Add Impedance Transformer option is provided when the parameters of a MJSS, MJSR, MLSS or MLSR command are edited in an Artwork view. The output side junction element is edited here.

Opens and impedance transformers (*ZDBL* and *ZHALF*) are required in the single-ended equivalent for a symmetrical combination network (see Figure 1). When explicit T-junctions or crosses are used, options can be set to obtain the behaviour required. The Convert to Open option is provided with MJIS, MJOS, MLIS and MLOS commands (refer to Figure 6), while the Add Impedance Transformer option is provided with MJSS, MJSR, MLSS and MLSR commands (refer to Figure 7).

An example of using the open and transformer options is provided in Figure 8. The Open and Transformer options were set for the T-junctions marked in dark grey in this figure. These T-junctions are symmetry points in the single-ended equivalents for the symmetrical input and output combination networks. Note that the schematic symbols associated with a modified T-junction are changed to flag the modifications to the commands. (See the insets in Figure 8.)

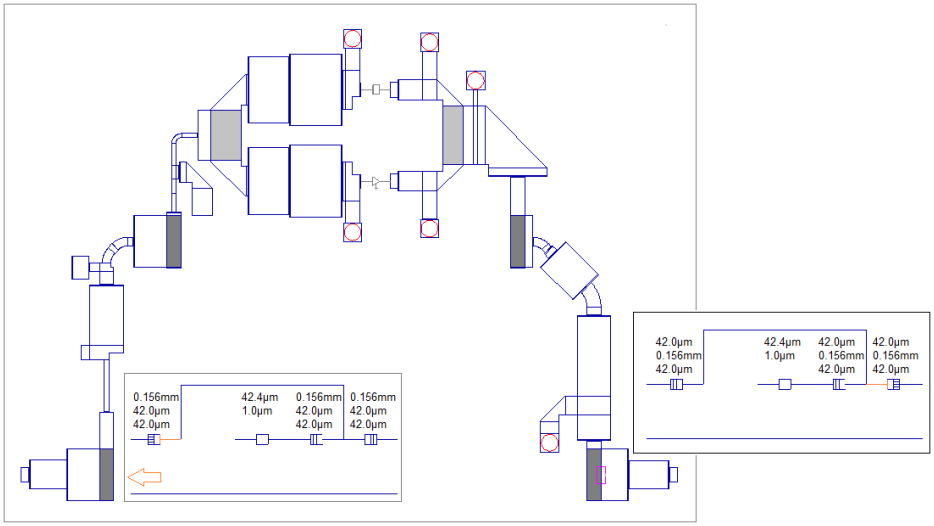

Figure 8. Open and Impedance Transformer options were set for the relevant junction elements at the symmetry points marked in dark grey. These options can also be set for the light grey junctions to open the voltage-shunt feedback path.

The matching networks in Figure 8 were synthesized by using the phase-controlled conjugate-match ADW synthesis features (CMA networks). The optimization features provided in the ADW were also used extensively. The impedance-matching targets were set by using the ADW power contour and maximum efficiency area capabilities. The second harmonic impedances in the circuit designed are also well-behaved. (Note that the power performance cannot be controlled directly in the MW.)

Two stages are connected in parallel in Figure 8 by using a voltage-shunt feedback block for the second stage. This was done to allow calculation of the loop gain associated with the two transistors connected in parallel (Sufficient gain and phase margins are required to avoid odd-mode oscillation). During the initial phases of the design the voltage-shunt feedback can be removed by using the Open and Transformer options associated with the T-junctions shown in light grey. (Note that the loop gain cannot be calculated in the MW.)

The symmetrical circuit associated with the single-ended equivalent in Figure 8 is shown in Figure 9. The electrical behaviours of the symmetrical sections in the assembled circuit are identical.

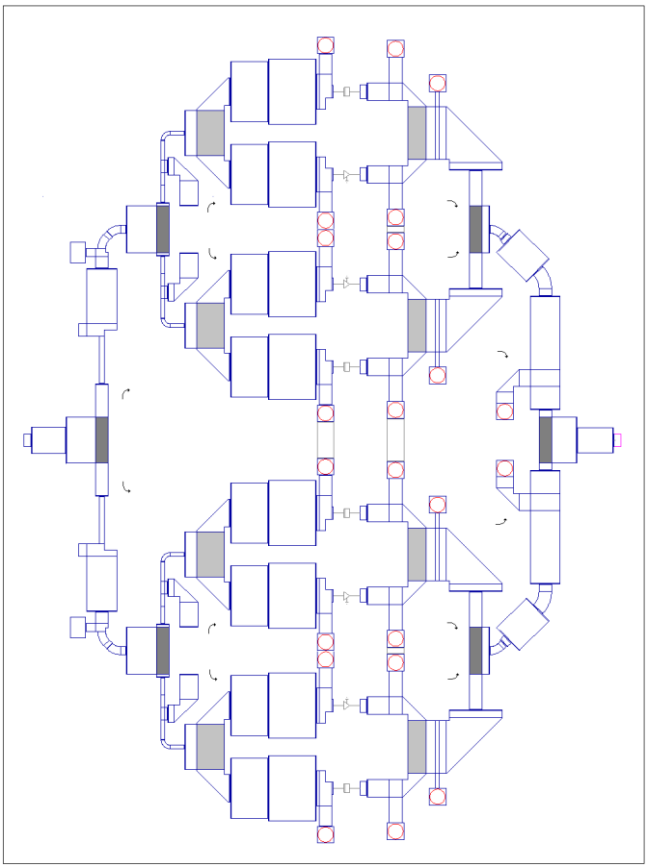

Figure 9. The symmetrical circuit associated with the single-ended circuit in Figure 8.

Note that the rotation directions in the artwork shown in Figure 9 are opposite for adjacent sections. The required rotation can be obtained by editing the exported ADW/MW artwork in Microwave Office™. Alternatively, a copy of the ADW/MW single-ended circuit can be created, and the artwork can be rotated in the ADW/MW. The rotated circuit can then be exported to Microwave Office™ too.

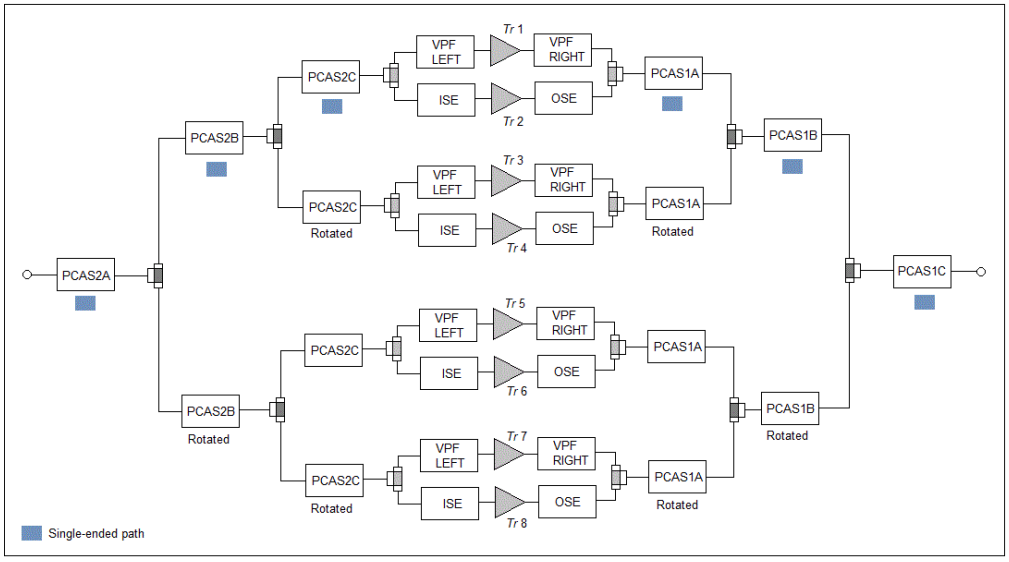

Figure 10. Assembly information for the ADW/MW circuit exported to Microwave Office™.

Assembly information for the ADW/MW circuit exported to Microwave Office^{TM} is provided in Figure 10. Before assembling the symmetrical amplifier, the two combination networks (PCAS2 and PCAS1) were each separated into three sections (PCAS2A, PCAS2B, PCAS2C; PCAS1A, PCAS1B, PCAS1C). The sections are defined by the T-junctions at the symmetry points. These junctions are not used in the Microwave Office sections created and were moved to the top schematic.

The voltage-shunt feedback networks were separated into two sections VPF LEFT and VPF RIGHT. The set of two-port parameters (transistor parameters) used in the ADW/MW VPF network separates the two sections.

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References

1. E. Hammerstad, “Equations for Microstrip Circuit Design”, Proc. 5th European Microwave Conference, September 1975.

2. Gopinath, A., et al, “Equivalent Circuit Parameters of Microstrip Step Change in Width and Cross Junctions”, IEEE Trans., Vol. MTT-24, 1976, pp. 142-144.

