

THE MULTIMATCH DESIGN PHILOSOPHY

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1. INTRODUCTION

The MultiMatch Amplifier Design Wizard is the result of twenty three years of intensive development. As it stands at the moment, the results obtainable with the Amplifier Design Wizard greatly surpass those which are readily obtainable with other synthesis and/or optimization approaches. Because of the concentrated power, design cycles are reduced to a fraction of the time previously required.

2. THE CONVENTIONAL APPROACH TO DESIGNING RF AND MICROWAVE CIRCUITS

The prevalent approach to the design of RF and microwave circuits today is still the optimization approach. An initial solution is obtained by some means or other, and this solution is “optimized” (improved by using optimization techniques) with a general-purpose RF and microwave circuit simulator. This approach has the following disadvantages:

- C The optimization as provided in most circuit simulators is limited to a specific pre-defined topology.
- C A circuit (amplifier) is usually optimized as a whole. It is not systematically put together (synthesized) in a step by step process.
 - In some cases, a single-frequency circuit is synthesized systematically for use as the initial solution in a broadband design, but there is no guarantee that the specific circuit chosen is the optimum, or even a good choice, for the wide-band problem.
- C Optimization problems are subject to the phenomenon of local minima and, therefore, the initial values assigned to the components. Even with a fixed topology, the chances of finding the global optimum to a practical, non-trivial microwave optimization problem are often poor.

- C The optimum targets for the problem to be optimized are not known, at least not initially.
- C Because only a single solution is optimized, no perspective is obtained on the problem solved.

While this approach is certainly workable, it is slow, depends heavily on the experience of the designer (or some other source), and usually yields inferior results. The requirement of initial solutions is also a major drawback.

3. DESIGNING CIRCUITS BY DOING SYNTHESIS-BASED SYSTEMATIC SEARCHES

In MultiMatch the basic point of departure is that one cannot rely only on optimization techniques to find close-to-optimum solutions. A solution to this problem is to find solutions by doing systematic searches. A simple grid search is, however, not the answer. In order to do the required search efficiently, the search must, in the first place, be done on the correct parameters and, secondly, it should be synthesis based. A number of the best solutions found in the systematic search are then optimized, after which the user can choose the best solution from the potential solutions presented.

Note that the systematic searches also eliminate the initialization problem.

3.1 IMPEDANCE MATCHING WITH MULTIMATCH

When impedance-matching networks are synthesized, the transformation Q s, as defined in [1], were found to be excellent parameters for a systematic search. Similar to the Q of a circuit, these Q s are inherently constrained in range, and the step size can be chosen realistically without significantly reducing the probability of finding close-to-optimum solutions. The last two transformation Q s in a network are constrained further by synthesizing the network to approximate the specified gain at least one of the frequencies in the passband (a gain window is set for this purpose). The efficiency of the search can also be increased by doing a coarser main search combined with finer searches around a number of the best solutions (usually 10 to 25) obtained in the main search. The best solutions obtained are then optimized with a steepest-gradient optimization routine (random optimization is, in principle, not used).

It is important to realize that the searches done are topology independent. It is, however, a simple matter to constrain the search on the transformation Q s to result in a wide variety of practical topology constraints. Some of the constraints which are allowed in MultiMatch are to limit solutions to:

- C Lowpass form.
- C High-pass form.
- C Networks without any series capacitors.
- C Networks without any shunt inductors.
- C Networks suitable for biasing purposes.

Constraints on the characteristic impedances, the line lengths and the values of any lumped components were also implemented. The option to replace shunt capacitors with shunt overlay capacitors is also provided.

The MultiMatch impedance-matching modules can synthesize

- C Lumped-element matching networks (SynL).
- C Commensurate (equal line lengths) distributed matching networks (SynC).
- C Non-commensurate distributed matching networks (SynL).
- C Mixed lumped/distributed matching networks (SynL).

Note that the algorithms implemented in SynC were generalized so that different lengths can be used for the main-line sections, the open-ended stubs and the short-circuited stubs. By using short stubs, the option to replace any stub with an equivalent stub, or a lumped component with pads, is introduced (if the line length is short, the tangent function is essentially linear).

Matching networks for power transistors are often designed without using any stubs. This can now also be done in SynL by using the following options:

- C Choose the topology option not to have any shunt inductors (short-circuited stubs).
- C Choose the option to replace any open-ended stubs with double stubs when the distributed*microstrip parameters are specified.
- C Choose the option to replace double stubs with stepped main-line sections.

When mixed lumped/distributed matching networks are synthesized, the line lengths are reduced by using lumped elements. Constraints can also be imposed on the lumped elements for this purpose (From the viewpoint of accuracy, a short line or stub is preferable to a lumped component). The pad size to be used with each type of lumped component (series*shunt capacitors*inductors) must be specified by the user. In order to minimize the parasitics introduced, any pads specified should be as small as possible.

All of the matching networks are synthesized to approximate the specified transducer power gain versus frequency response between two specified complex terminations. The specifications must be provided in ~~##~~real-frequency~~##~~ format (terminations and gain specified at a number of frequencies in the passband of interest). No equivalent circuits or an analytical expression for the gain response is required, or used. In the Amplifier Design Wizard, the gain at each frequency can be specified to be less than, greater than or equal to the gain value specified. The less than option is useful

when rejection is required.

In order to evaluate the relative sensitivity of the different solutions to component changes, a worst-case tolerance analysis is done on each network in the results section of the relevant impedance matching module. The default tolerance value is 1%.

The choice of the specific solution to be used is left to the user. Having several solutions to choose from (different topologies and different element values) is an advantage from a manufacturing viewpoint and also provides perspective on the problem being solved.

The option to create a MultiMatch circuit file for the solution chosen, or to insert the solution chosen at a marked position in a previously created circuit file, is provided on leaving the results section of the impedance-matching modules.

Microstrip capability

MultiMatch synthesizes networks electrically, that is, in terms of inductance, capacitance, resistance, characteristic impedance and electrical line length. If microstrip or stripline solutions are required, these electrical solutions must be transformed and optimized before they are of practical use. A distributed MultiMatch circuit can be transformed automatically into microstrip or stripline form, with the option to adjust the line lengths to compensate for the shifts in the reference planes caused by step, tee and cross junction discontinuities. Step junctions can also be tapered to reduce the associated discontinuity effects. If suitable values were chosen for the characteristic impedances, the performance of the transformed circuit usually corresponds closely to that of the original circuit, even when complete amplifier circuits are transformed. The characteristic impedances should be chosen to minimize any transformer effects or reactive loading effects at the different junctions. The information required to make an appropriate choice is provided when required.

It should be realized that the discontinuity effects decrease as the substrate height is decreased. Too thin lines could, however, result in unacceptable conductor losses.

A MultiMatch circuit can be exported in Super Compact™ or Touchstone™ netlist format, or as a Microwave Office™ script (This script can be run in Microwave Office™ to create the schematic). Any remaining discontinuity effects can then be reduced by optimization in Microwave Office or in a simulator that can import the Super Compact or Touchstone netlists. DXF files can also be exported and these can be imported into an EM simulator. If the circuit is optimized externally, the two-port parameters of the optimized network can be imported again into MultiMatch (**##.s2p** format). This approach is also followed when circuits are realized on media other than microstrip or stripline (co-planar, suspended substrate or waveguide circuits are not yet supported in MultiMatch).

Note that a MultiMatch circuit can be exported in electrical or geometrical format. The electrical circuit description can be used as target for any external microstrip*stripline optimization required. Depending on the substrate height and the

accuracy level, MultiMatch microstrip*stripline circuits are usually adequate up to at least 12GHz.

Any components not presently supported in MultiMatch (like radial stubs, interdigital capacitors, spiral inductors, ...) can also be designed with another software tool, after which it can be imported into MultiMatch in terms of its *S*-parameters and noise parameters. Note that spiral inductors can usually be modeled adequately in MultiMatch as an ideal inductor with pads and parasitics.

The Equivalent Passive Problem

The best way to synthesize an amplifier is to control the available power gain and the noise figure, or the operating power gain and the output power, of each stage in the amplifier sequentially. The design should be started at the source side in the low-noise case, and at the load side when the output power is of interest. If this approach is followed, the input or the output terminals of the (modified) transistor used must be presented with a set of impedances which lie on or near to the circumference of the different constant gain circles * constant noise figure circles * constant power contours of interest. An impedance-matching network must, therefore, be synthesized to transform the existing impedances to those required at the different frequencies of interest.

If the transistor is inherently stable or was compensated to be so [1, 2], it is possible to transform each of the circle problems (constant gain or constant noise figure circles) to a passive impedance-matching problem which is exactly equivalent (Inherent stability is not required when the noise figure is controlled). To understand how this is possible, it is only necessary to realize that the problem of matching a passive source to a passive load is also a circle problem when the required transducer power gain is less than unity [1, 2]. The active problem then simply reduces to finding the passive problem for which the circle required is exactly the same as the constant noise figure circle * constant gain circle of interest.

In those cases where inherent stability was not established or when the output power is controlled (elliptic contours), the optimum point on the relevant circle or power contour can be selected to complete the specifications for the equivalent passive problem. The option to enforce such a "point-match" is also provided in the inherently stable case. Note that, when a circle-match is possible, a point-match should only be enforced if the performance is only acceptable over a small segment of the relevant circle.

3.2 DEVICE MODIFICATION

The capability to solve impedance-matching problems and the concept of the equivalent passive problem are critical factors in establishing a general amplifier synthesis capability. However, it will be found that these alone do not bring one very far. The following problems, all of which are associated with the transistor(s) to be used, still need

to be solved:

- C Stability outside the passband can be a major problem. Synthesizing a network that will provide the required performance inside the passband and that will ensure stability outside the passband can be difficult. When it can be done, unnecessary constraints are imposed on the performance inside the passband.
- C All non-trivial impedance-matching problems have inherent gain-bandwidth constraints. If these constraints are too severe and cannot be reduced, the bandwidth can only be increased by degrading the associated VSWR (that is, when a lossless matching network is used).
- C Transistors have inherent gain slopes at higher frequencies. While these gain slopes can be removed with lossless networks with suitable positive slopes, the sensitivity resulting from such networks is frequently a problem.
- C The optimum noise figure*optimum power termination for a transistor is usually very different from the optimum gain termination.

The answer to these problems is to add frequency-selective, resistive, feedback and/or loading networks to the transistor. In doing so, a ~~new~~ transistor is created which is more suitable to the application at hand. This class of action will be referred to as device modification. Two series of modification techniques were developed and are implemented in MultiMatch.

3.2.1 GAIN SLOPE CONTROL WITH LOSSY SECTIONS

In the first series of modification techniques implemented in MultiMatch, a table of the components required to provide a specified slope in the maximum available power gain (MAG) or the maximum stable power gain (MSG) is created. (To understand why the MAG is targeted, is it necessary to understand that a flat gain response and low input and output VSWRs can only be obtained with lossless matching networks if the MAG of the transistor has been leveled first). Tables can be created for

- C Voltage-shunt feedback sections.
- C Current-series feedback sections.
- C Shunt loading sections.
- C Series loading sections.

In each case, the gain slope is controlled with a resistor used in combination with some lossless component(s). (In the simplest case, a resistor is used in parallel with a capacitor, or in series with an inductor). By using a lossy network to reduce the gain slope, the stability and the VSWRs may be improved simultaneously. In general, sensitivity is also not a problem. This follows because these networks usually have Q s which are low in comparison with those required from an equivalent lossless network.

Note that the MSG can only be controlled when a feedback section is synthesized. If the slope in the MAG is set to be equal to that in the MSG, tables of the components required to stabilize the transistor at different gain levels can be created too.

Different gain slope control sections can be combined sequentially. Some fraction of the gain slope can first be removed with one section, after which a second section can be used to level the gain. The first section can be used to control the MSG or the MAG, while the second is usually used to level the MAG. Note that if feedback sections, as well as loading sections are used, the feedback must be applied before the loading.

Better VSWRs can often be obtained when two sections are combined to reduce or to level the slope in the MAG. At least two modification sections are usually required for good results.

3.2.2 THE DOUBLE-SECTION MODIFICATION TECHNIQUES

In the second series of modification techniques implemented in MultiMatch, any two of the different modification sections (voltage-shunt feedback, current-series feedback, shunt loading and series loading) are combined automatically to level the gain of the stage synthesized. While only the MAG or the MSG could be controlled with one of the single-section modification networks, any of the following gain functions can be controlled with a double-section modification network:

- C The MAG.
- C The MSG.
- C The transducer power gain (G_T).
- C The available power gain (G_a).
- C The operating power gain (G_w).
- C The available power gain associated with the optimum noise figure of the modified transistor (G_{anopt}).

The performance of any stages synthesized previously (multistage amplifier) are taken into account when the gain is controlled.

The networks synthesized are optimized first before the solutions are presented to the user. Optimization is in terms of an error function, through which control is provided over the following parameters:

- C The average power gain over the passband.
- C The gain ripple.
- C The highest input VSWR and output VSWR in the passband.
- C The highest noise figure in the passband.
- C The degree of difficulty of the noise match, expressed as a VSWR.
- C The lowest output power in the passband.
- C The lowest Rollette stability factor in the passband or over the complete frequency range over which S -parameter data were provided for the transistor.

Note that the VSWR targeted could be an actual VSWR (like the final input VSWR) or could be a VSWR used to indicate the degree of difficulty of the matching problem to be solved. To appreciate this, consider the case where the MAG is controlled. If perfect matching networks could be designed, the input VSWR, as well as the output VSWR, would be unity when the matching networks are in place. The poorest VSWR in the passband before a matching network is added to the circuit, is used as an indication of the degree of difficulty of the associated matching problem. The VSWR is calculated in terms of the actual source * load impedance in place before the matching network is added.

It is important to realize that when the MAG, G_a , G_w or G_{anopt} is controlled, a conjugate match at the other port of the modified transistor is implied. This implies that a matching network is required on this port before the performance targeted can be realized. No matching networks are required when the transducer power gain (G_T) is controlled. When G_{anopt} is controlled, an optimum noise match is required on the input side and a conjugate match on the output side.

Contrary to popular believe, excellent low-noise stages can usually be synthesized by using lossy sections. Such sections should, however, be used on the output side of the transistor. The best low-noise results are usually obtained by synthesizing the modification section to control G_{anopt} or the MAG. Similarly, modification is usually done on the input side of the transistor when the output power should be maximized.

Similar to impedance-matching networks, the double-section modification networks are synthesized by doing a synthesized-based systematic search. The search is done over all networks which provide the specified gain at least one of the passband frequencies. A number of the best solutions (up to 45) are stored and optimized with a steepest-gradient optimization technique. The search can be constrained not to include voltage-shunt feedback sections (this is useful when packaged transistors are used at higher frequencies), or it can be done for a specific combination of the modification sections. As in the case of impedance matching networks, the choice of the specific modification network to be used is left to the user.

In earlier versions of MultiMatch, no provision was made for connecting lines or for the pads required for the lumped components when modification networks were synthesized. This was found to be a major drawback and was corrected in the

optimization phase of the synthesis cycle. Because of the optimization step, one-port parasitics are also allowed for the lumped components. Note that unaccounted parasitics can have a disastrous effect on the expected performance of a voltage-shunt feedback loop.

3.2.3 STABILITY CONSIDERATIONS

A complete picture of the relative stability of a (modified) transistor is not provided by the k factor (Rollette stability factor) typically used for this purpose. It has been found that the loop gain associated with each feedback loop should be evaluated too. Although the loop gain is dependent on the terminations used, it provides the information and the control required to handle most stability problems. Note that ignoring the information provided by the k factor is not advocated. The loop gain of a circuit can be evaluated in the MultiMatch Analysis Module.

Any potentially unstable two-port ($k < 1$) can be stabilized by loading its input and/or output terminals with series or shunt resistance (Loading on both sides is sometimes required). Stabilization is sometimes also possible with a voltage-shunt feedback resistor. Valuable insight into the degree of instability is often gained from the values of the stabilizing resistance required. Tables of the resistance required are, therefore, also created in the Device-Modification Module for the different modification options. When resistive loading (series or shunt) is used, values for the components required to provide the required stabilizing resistance at the edges of the band over which the transistor is potentially unstable, are also listed (that is, if possible).

4. CONTROLLING THE OUTPUT POWER OF AN AMPLIFIER OR AN OSCILLATOR IN MULTIMATCH

The output power (P_{out}) or the effective output power ($P_{out}|P_{in}$) of an amplifier or an oscillator is often an important design parameter. Incorporating the power as a synthesis parameter in MultiMatch was a major step in its development. In MultiMatch, power control is based on the fact that the fundamental tone output power of a linear amplifier is mainly determined by the level at which the intrinsic output voltage and/or the intrinsic output current of the limiting transistor starts to clip. This principle is used to estimate the 1 dB compression point of each transistor, as well as to generate contours of constant output power or effective output power for each transistor. Correlation between the predicted and the actual results has been found to be excellent for class A amplifiers, as well as class B amplifiers.

In order to calculate the power parameters [2] required to estimate the output power of a circuit, a small-signal model of the transistor and the I/V-plane load-line boundaries are required. In MultiMatch, the load-line boundaries are defined by four

boundary lines and the dc operating current and voltage. (The operating point is also the bias point in class A amplifiers.) The small-signal model can be extracted from the specified small-signal S -parameters in the MultiMatch S -parameter Module or in the Analysis Module. For accurate modeling of the current and voltage clipping, the model should closely represent the actual transistor, that is, in topology, as well as component values.

When the power performance of a multi-stage amplifier is calculated, the influence of each transistor on the power performance is established. This is done by assuming that clipping occurs in only one transistor at a time, with the other transistors ideal. The output power of each stage is referenced to the load. Optimization power margins can be specified for the drivers, thereby ensuring that the output power will be limited mainly by the load stage. This feature also allows greater control on the intermodulation distortion.

5. THE CIRCLE AND POWER MODULES

The MultiMatch impedance-matching modules were designed to solve passive impedance-matching problems. An active matching problem is converted to the equivalent passive impedance-matching problem in the MultiMatch Circle * Power Module. Any one of the following parameters can be set as target in the Circle * Power Module:

- C The operating power gain (G_w).
- C The available power gain (G_a).
- C The transducer power gain (G_T).
- C The noise figure (F).
- C The output power (P_{out}).
- C The effective output power (P_{out} / P_{in}).

The specifications set for the stage designed correspond to one of the following:

- C A set of constant gain circles.
- C A set of constant noise figure circles.
- C A set of constant power or effective power contours.

The performance around these circles * contours can be evaluated extensively before finalizing the choice of the optimum point on each of the circles * contours (or choosing a different set). An error function is used to decide on the default optimum point on each circle or contour. The parameters of this error function can be modified by the user when the summary table is displayed. The summary table is displayed directly after the specifications for the performance required are made and summarizes the potential performance on the circles * contours targeted. (The variation of the best and the worst performance on each circle*contour, over the passband of interest, is displayed.)

The circles * contours of interest can be displayed graphically in the results section of the Circle * Power Module. The performance around each circle * contour can also be displayed numerically in a table. Zoom capabilities are provided in these tables in order to allow displaying of the performance at any point on the circle * contour of interest. The following parameters are displayed in the tables:

- C The power gain (G_a , G_w or G_T) on a constant noise figure circle or a constant output power contour, or the noise figure (F) around a constant gain circle or a constant output power contour. When the operating power gain (G_w) or the output power (P_{out}) is controlled, the noise figure associated with a conjugate match on the input side, or with the termination currently in place on the input side, is calculated.
- C The degree of difficulty of the associated impedance-matching problem expressed as a VSWR. The required impedance is compared with the impedance actually in place when this is done.
- C The Sterne stability factor with the stabilizing influence of the terminations taken into account.
- C The tunability factor.

The tunability factor is a measure of the influence that any impedance changes (tuning) on the output * input side of the transistor will have on the impedance at the other side. When the input and the output sides of a transistor are perfectly isolated (unilateral case), the tunability factor is zero. A tunability factor of less than 0.3 is usually acceptable. Note that ~~poor~~ tunability is an advantage when the input VSWR of a low-noise stage or the output VSWR of a power stage is controlled by the termination on the other side of the (modified) transistor (VSWR control via s_{12}).

- C Worst-case sensitivity factors associated with variations in the controlling admittance. A default tolerance of 1% in the controlling admittance is assumed when these sensitivity factors are calculated. Sensitivity factors are calculated for the noise figure (δ_n), as well as the gain (δ_g).
- C The available power gain (G_a) * operating power gain (G_w) specified can only be extracted as actual gain if the output impedance (G_a) * input impedance (G_w) of the transistor is conjugately matched to the load (G_a) * source (G_w). Assuming that this will (and can) be done, an output VSWR (G_a) * input VSWR (G_w) of unity is, therefore, expected after matching. Any tolerance in the controlling admittance presented to the input terminals (G_a) * output terminals (G_w) of the (modified) transistor will degrade this match. The worst-case deviation in the expected VSWR (δ_{vs}) is calculated and listed with the other sensitivity factors. The

tolerance circle used for the gain * noise figure sensitivity factor is also used for the VSWR sensitivity factor.

A data file for the equivalent passive impedance-matching problem to be solved is created automatically on leaving the Circle * Power Module. The problem is then solved with one of the impedance-matching modules. Note that the problem is solved in terms of the equivalent passive problem. The option to optimize the networks synthesized in terms of the active performance is provided in the results section of SynL or SynC. The targets as each frequency can again be set to be less than, greater than or equal to the value specified.

6 ARTWORK GENERATION

As described above, the basic artwork for the circuit is generated automatically from the electrical circuit description. Extensive graphical manipulation of the microstrip artwork is possible. This includes the following:

- C Flipping stubs around.
- C Adjusting the gap spacing or offsets vector used for a lumped component.
- C Adjusting the dimensions of a line.
- C Bending a line (optimum mitre).
- C Curving a line.
- C Meandering a line.
- C Tapering a step junction.
- C Closing any mis-aligned voltage-shunt feedback loop or series block loop (two cascade networks connected in parallel) automatically. A suitable component must be selected before the loop is closed.

When a line is bent or curved or meandered, the physical line length is adjusted to keep the electrical line length unchanged. This is also done when step junctions are tapered.

A Super Compact[™] or a Touchstone[™] nodal description for the MultiMatch artwork is created when the artwork is displayed. If necessary, the microstrip * stripline performance can be verified by analyzing the circuit with an accurate circuit simulator that can import either of these formats. Any residual discontinuity effects can then also be removed by optimization before the circuit is manufactured. Any elements not available in MultiMatch can also be added at this stage. MultiMatch circuits can also be exported to Microwave Office. The script created by MultiMatch can be executed in Microwave Office to create the schematic of the circuit.

DXF or HPGL files can also be created for the MultiMatch artwork. The DXF artwork can be used for electromagnetic simulation of the microstrip networks designed in MultiMatch.

7 OPTIMIZATION BY RE-SYNTHESIS

The matching and modification networks selected during the design process may not necessarily be the best. Furthermore, if the transistor(s) used is highly non-unilateral, the match provided by the first matching network synthesized (the input or the output matching network) may have deteriorated. It is usually also possible to improve the input match of a low-noise stage by re-synthesizing the load network of the input stage (first inter-stage network) to mismatch the output impedance of this stage to the rest of the amplifier. Similarly, the output match of a power amplifier can usually be improved by re-synthesizing the first inter-stage network on the output side.

The performance of the synthesized circuit can be improved by re-synthesis, or by using the optimization features provided in the Analysis Module, the Device-Modification Module and the results sections of the Impedance-Matching Modules. The topology will, however, not be changed when the circuit is optimized directly. In order to allow for topology changes, a series of Impedance-Matching Wizards are provided in the Analysis Module. These wizards can be used to re-synthesize any specific (cascade) matching network, or any modification network. The circuit is split into two sections (a left-hand side or input section, and a right-hand side or output section) at the insertion point of the new matching network or the transistor and the associated modification network. The Two-port Command on the Schematic Toolbar can be used to replace any of the transistors used in the circuit with a different transistor, or the same transistor at a different bias point, if necessary.

The wizards provided in the latest version of MultiMatch are listed below, with a description of the function of each wizard.

General Impedance-Matching Wizard

The IIM, RMT, LMT and NOI commands can be activated by using this wizard. The different commands are described below:

IIM

This command is used to set up an interstage impedance-matching problem. It can also be used to set up the problem associated with improving the input or the output match of the circuit.

The terminations for the left-hand side section of the circuit (section on the input side of the insertion point) are taken to be the actual source terminations of the circuit (as defined in the terminations block of the circuit file), while that for the right-hand side section is taken to be the actual load terminations.

RMT

The RMT command also sets up an interstage impedance-matching problem, but

instead of using the actual load terminations as load terminations for the section to the right of the insertion point, the terminations associated with the MAG (maximum available gain) of that section is used.

LMT

The LMT command is similar to the RMT command, but the input side of the section to the left of the insertion point is terminated in its MAG terminations.

NOI

The NOI command is used to minimize the noise figure of the circuit section to the right of the insertion point (the output section). The circuit is assumed to be terminated as specified in the circuit file.

IVI Wizard

This wizard is used to set up an interstage impedance-matching problem to improve the input VSWR of the section to the left of the insertion point by mis-matching its output impedance to the input impedance of the section to the right of the insertion point. It is frequently use to improve the input VSWR of a low-noise amplifier. The gain of the amplifier can usually be leveled at the same time.

OVI Wizard

This wizard is similar to the IVI Wizard and is used to set up an interstage impedance-matching problem to improve the output VSWR of the section to the right of the insertion point by mis-matching its input impedance to the output impedance of the section to the left. As in the IVI case, the gain of the amplifier can usually be leveled at the same time.

CIL Wizard

This wizard is used to (re-)design an interstage network to control the output power (P_{out}) or the operating power gain (G_w) or the transducer power gain (G_T) of the section to the left (on the input side) of the insertion point.

CIR Wizard

This wizard is used to (re-)design an interstage network to control the noise figure (F) or the available power gain (G_a) or the transducer power gain (G_T) of the section to the right (on the output side) of the insertion point.

MOT Wizard

This wizard is used to (re-)synthesize a new modification network or to replace the

current (modified) transistor in an amplifier stage. It sets up the information required by the Device-Modification Module to insert a new stage (a transistor with its modification networks) at the insertion point.

8 REFERENCES

1. Pieter L.D. Abrie, The Design of Impedance-Matching Networks for Radio-Frequency and Microwave Amplifiers, Artech House, Inc., 1985.
2. Pieter L.D. Abrie, Design of RF and Microwave Amplifiers and Oscillators, Artech House Inc., 1999.